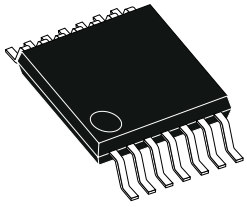
STEF01

Datasheet

8 V to 48 V fully programmable universal electronic fuse



HTSSOP14

Maturity status link	
STEF01	
Device summary	
Order code	STEF01FTR
Package	HTSSOP14
Packing	Tape and reel

Features

- Operating input voltage range: 8 to 48 V
- Absolute maximum input voltage: 55 V
- Continuous current typ.: 4 A
- N-channel on-resistance typ.: 30 mΩ
- Enable/fault functions
- Output clamp voltage: adjustable from 10 to 52 V
- Programmable undervoltage lockout
- Short-circuit current limit
- Programmable overload current limit
- Adjustable soft-start time
- Latch or auto-retry thermal protection
- Maximum allowable power protection
- Power Good
- Drives an optional external reverse current protection MOSFET
- Operating junction temperature -40 °C to 125 °C
- HTSSOP14 package

Applications

- Hot board insertion
- Electronic circuit breaker/power busing
- Industrial/alarm/lighting systems
- Distributed power systems
- Telecom power modules

Description

The STEF01 is a universal integrated electronic fuse optimized for monitoring output current and the input voltage on DC power lines.

When connected in series to the main power rail, it is able to detect and react to overcurrent and overvoltage conditions. When an overload condition occurs, the device limits the output current to a safe value defined by the user. If the anomalous overload condition persists, the device goes into an open state, disconnecting the load from the power supply.

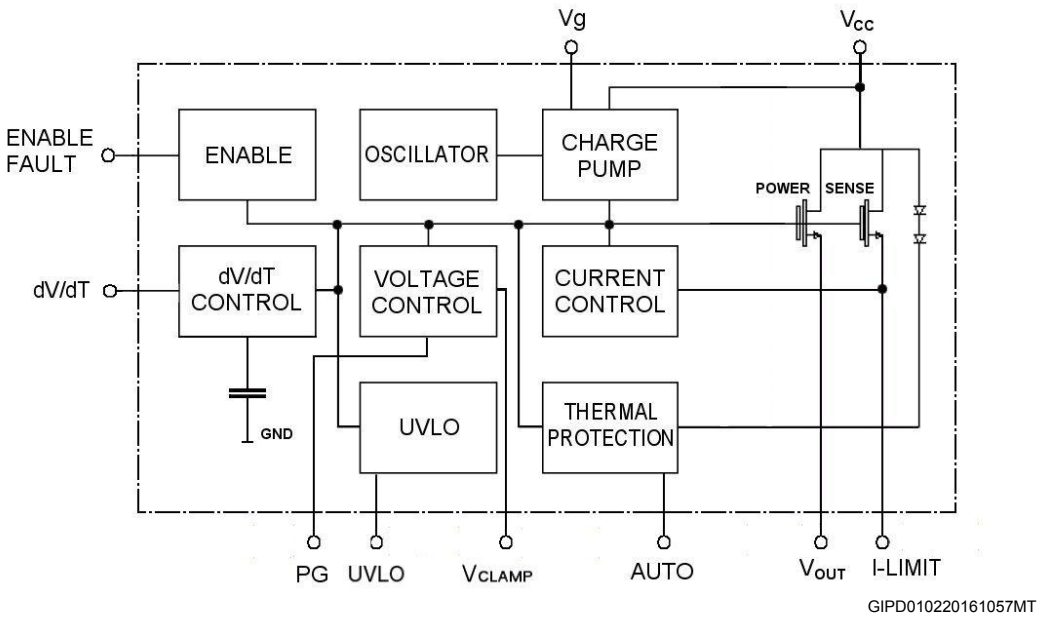
The device is fully programmable. UVLO, overvoltage clamp and start-up time can be set by means of external components.

The adjustable turn-on time is useful to keep the in-rush current under control during startup and hot-swap operations. The device provides either thermal latch and auto-retry protection modes, which are selectable by means of a dedicated pin.

The STEF01 provides a gate driver pin for an external power MOSFET to implement a reverse-current blocking circuit. The intervention of the thermal protection is signaled to the board monitoring circuits through a signal on the fault pin.

1 Device block diagram

Figure 1. **Block diagram**



2 Pin configuration

Figure 2. **Pin configuration (top view)**

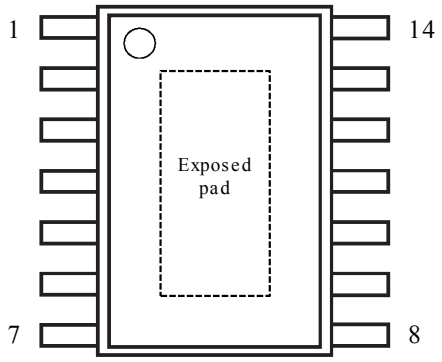


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Table 1. **Pin description**

Pin n°	Symbol	Note
1	UVLO	A resistor divider connected between this pin, Vcc and GND sets the UVLO threshold. If left floating the UVLO is preset to 14.5 V.
2	dv/dt	The internal dv/dt circuit controls the slew rate of the output voltage at turn-on. The internal capacitor allows a ramp-up time of around 3 ms. An external capacitor can be added to this pin to increase the ramp-up time. If an additional capacitor is not required, this pin should be left open.
3	GND	Ground pin.
4	Auto	This pin selects the thermal protection behavior. The device is set in latched mode when this pin is left floating or connected to a voltage higher than 1 V. It is set in auto-retry mode when the pin is connected to GND.
5	Vclamp	A resistor divider connected between this pin, V_{OUT} and GND sets the overvoltage clamp level. If left floating the clamp is preset to 28 V.
6, 7, 8, 9	V_{OUT}	Output port. All the pins must be tied together with short copper tracks.
10	I-Limit	A resistor between this pin and V_{OUT} sets the overload current limit level.
11	Vg	Gate driver output for the optional external reverse-blocking MOSFET.
12	En/Fault	Tri-state, bi-directional pin. During normal operation the pin must be left floating, or it can be used to disable the output of the device by pulling it to ground using an open drain or open collector device. If a thermal fault occurs, the voltage on this pin will go to an intermediate state to signal a monitoring circuit that the device is in thermal shutdown. It can be connected to another device of this family to cause a simultaneous shutdown during thermal events.
13	PG	Power Good flag. It is an open drain, to be pulled up through an external resistor.
14	V_{CC}	Input port. Connect this pin to the exposed pad.
Exposed pad	V_{CC}	Exposed pad. Input port of the device, internally connected to the power element drain.

3 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Positive power supply voltage	-0.3 to 55	V
V_{OUT}/source	Output voltage pin	-0.3 to V_{CC}	V
I-Limit	Current sense resistor pin	-0.3 to V_{CC}	V
I_D	Continuous current	6	A
PG	Power good flag pin	-0.3 to V_{CC}	V
Vclamp, UVLO	Vclamp, UVLO pins	-0.3 to 7	V
En/Fault	Enable/Fault pin	-0.3 to 7	V
dv/dt	Startup time selection pin	-0.3 to 7	V
Auto	Auto retry selection pin	-0.3 to 7	V
Vg	Gate driver pin	-0.3 to 65	V
T_J	Maximum junction temperature (1)	150	°C
T_{STG}	Storage temperature range	-65 to 150	°C
T_{LEAD}	Lead temperature (soldering) 10 s	260	°C

1. *The thermal limit is set above the maximum thermal rating. It is not recommended to operate the device at temperatures greater than the maximum ratings for extended periods of time.*

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 3. Recommended operating condition

Symbol	Parameter	Value	Unit
V_{CC}	Operating power supply voltage, steady state	8 to 48	V
	Maximum power supply voltage, clamping active	52	V
R_{Limit}	Current sense resistor range (1)	8 to 1000	Ω
I_D	Continuous current	4	A
T_J	Operating junction temperature	-40 to 125	°C

1. *Important: The R_{Limit} resistor is mandatory in the application. Very low values of the R_{Limit} or lack of connection of R_{Limit} may lead to malfunction of current limiting circuit and to device damage.*

Table 4. Thermal data

Symbol	Parameter	HTSSOP14	Unit
R_{thJA}	Thermal resistance junction-ambient, 2 layer PCB	140	°C/W
	Thermal resistance junction-ambient, 4 layer PCB	40	
R_{thJC}	Thermal resistance junction-case	4	°C/W

4 Electrical characteristics

V_{CC} = 24 V, V_{EN} = floating, C_I = 10 µF, C_O = 47 µF, T_J = 25 °C (unless otherwise specified).

Table 5. Electrical characteristics for STEF01

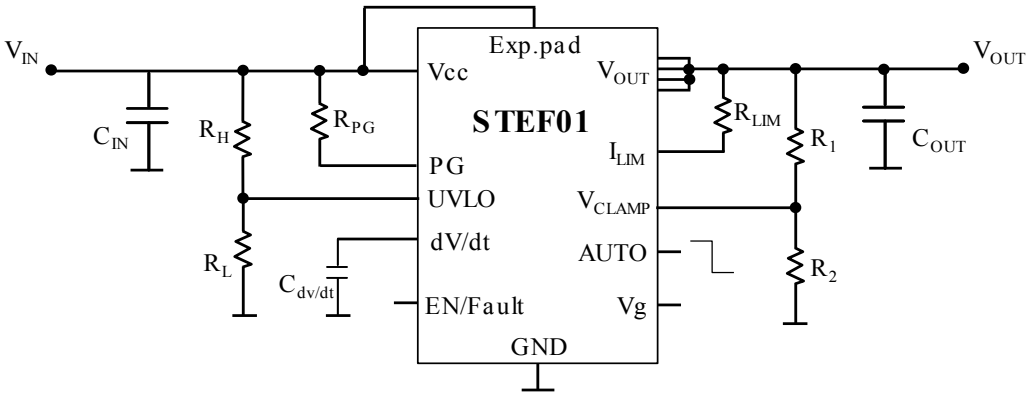
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Under/over voltage protection						
V_{Clamp}	Output clamping voltage	V_{CC} = 36 V, V_{Clamp} = floating		28		V
	Accuracy		-5		+5	%
	Output clamping voltage range	With external resistor divider on Vclamp pin	10		52	V
V_{ON}	Under voltage lockout threshold	Turn on, voltage going up, UVLO = floating	13	14.5	16	V
	Under voltage lockout range	With external resistor divider on UVLO pin	8		45	V
V_{Hyst}	UVLO hysteresis			10		%
Power MOSFET						
R_{DSon}	ON resistance	I_D = 1 A (1)		30	50	mΩ
		-40 °C < T_J < 125 °C (2)			70	
V_{OFF}	Off state output voltage	V_{CC} = 36 V, V_{GS} = 0, R_L = infinite		1	20	mV
Current limit						
I_{Short}	Short circuit current limit	R_{Limit} = 22 Ω, V_{OUT} = gnd		1.5		A
I_{Lim}	Overload current limit	R_{Limit} = 22 Ω, V_{OUT} = V_{CC} - 2 V, V_{CC} > 8 V	3.2	4	4.8	A
dv/dt circuit						
dv/dt	Output voltage ramp time	Enable to V_{OUT} = 22 V, No $C_{dv/dt}$		3		ms
		Enable to V_{OUT} = 46 V, V_{CC} = 48 V, V_{Clamp} = 52 V, no $C_{dv/dt}$		3.6		
$I_{dv/dt}$	dv/dt source pin current			100		nA
Enable/Fault						
V_{IL}	Low level input voltage	Output disabled		0.6		V
$V_{I(INT)}$	Intermediate level input voltage	Thermal fault, output disabled		1.4		V
V_{IH}	High level input voltage	Output enabled		2.6		V
$V_{I(MAX)}$	High state maximum voltage			5		V
I_{IL}	Low level input current (sink)	V_{Enable} = 0 V		-20	-40	µA
	Maximum fan-out for fault signal	Total number of chips that can be connected to this pin for simultaneous shutdown			5	Units
Power Good						
V_D	Power Good output threshold	V_{CC} - V_{OUT}value for Power Good		1		V
		Hysteresis		0.1		

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_L	Power Good output voltage low	I_{sink} = 6 m A open drain output			0.4	V
External MOS gate driver						
I_g	Sourcing current	Device on		30		µA
R_p	Strong pull down	V_{EN} = 0 V		450		Ω
V_g	Gate driver voltage	V_g-V_{OUT}	8.5	9.5	10.5	V
Auto-retry function						
V_{AR}	Autoretry logic level	Auto-retry activated			0.4	V
		Latched protection activated	1			
Total device consumption						
I_{Bias}	Bias current	Device operational		0.4		mA
		Thermal shutdown (2)		0.1		
		Off state (V_{EN} = GND)		0.1		
V_{min}	Minimum operating voltage				8	V
Thermal shutdown						
TSD	Shutdown temperature (2)			175		°C
	Hysteresis	Only in auto-retry mode		25		

1. *Pulsed test.*
2. *Guaranteed by design, but not tested in production.*

5 Typical application

Figure 3. **Application circuit**



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5.1 Operating modes

5.1.1 Turn-on and UVLO

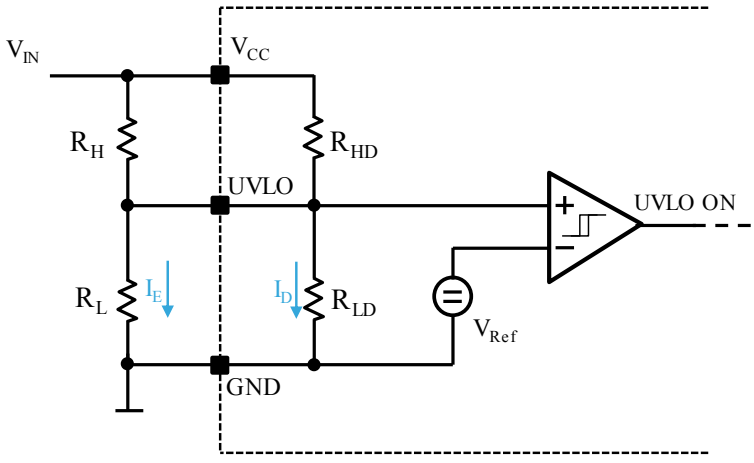
The device features a programmable UVLO block. If the input voltage exceeds the UVLO ON threshold (V_{ON}), the power pass element is turned on and the Enable/Fault pin goes up to the high state.

Figure 4. UVLO block simplified diagram shows the simplified diagram of the UVLO circuit. The voltage at the UVLO pin is compared to an internal 1 V reference (0.9 V during turn OFF).

The default ON threshold is set by internal divider (R_{HD}, R_{LD}) to 14.5 V; the I_D current flowing through the internal divider is set to ~ 3 µA.

The UVLO threshold can be modified in accordance with power rail needs by adding the R_H-R_L resistor divider, as shown in Figure 4. UVLO block simplified diagram. The external divider is in parallel with the internal default one, therefore the threshold can be changed within the 8 V to 45 V range.

Figure 4. **UVLO block simplified diagram**



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When the external divider is used, the ratio between external current I_E and the internal current I_D should be kept as high as possible, to guarantee maximum linearity of the circuit with respect to temperature and process variations.

Setting I_E/I_D > 10 provides sufficient UVLO linearity, at the same time keeping overall current consumption at acceptable levels. Given the desired V_{ON} threshold, for a fixed value of the lower resistor R_L, **Equation 1** can be used to calculate the upper resistor R_H.

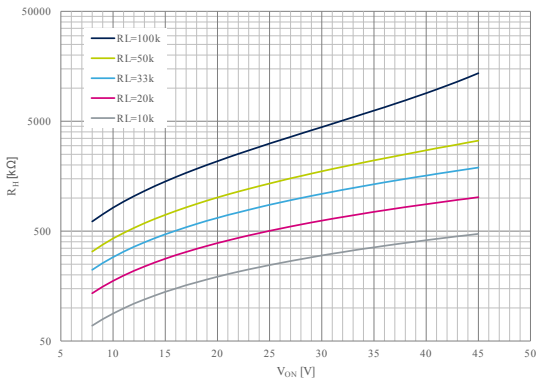
Equation 1

$$R_H = \frac{1}{\frac{(1/R_L + 1/333)}{(V_{ON} - 1)} - \frac{1}{4500}}$$

(resistor values are expressed in kΩ)

Figure 6. UVLO threshold (V_{ON}) vs R_H, R_L shows the relationship between R_H and the UVLO turn ON threshold, for some fixed values of R_L.

Figure 6. UVLO threshold (V_{ON}) vs R_H, R_L



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The resistor divider approach described above guarantees the best UVLO performance in terms of accuracy and temperature dependance.

In order to reduce the application B.O.M., the 1-resistor approach can be used also, at the expenses of overall UVLO circuit accuracy.

In this case, the R_H resistor can be omitted for V_{ON} thresholds higher than 14.5 V, or R_L for V_{ON} lower than 14.5 V.

In any case it is recommended to check that in all operating conditions, the UVLO threshold is never lower than 8 V, in order to guarantee correct operation.

After an initial delay time of typically 170 µs, the output voltage is supplied with a slope defined by the internal dv/dt circuitry. If no additional capacitor is connected to the dv/dt pin, the total time from the Enable signal going high and the output voltage reaching the nominal value is around 3 ms.

5.1.2 Normal operating condition

The STEF01 E-fuse provides the circuitry on its output with the same voltage shown at its input, with a small voltage fall due to the N-channel MOSFET RDS-on.

5.1.3 Output voltage clamp

If the input voltage exceeds the V_{clamp} value, the internal protection circuit clamps the output voltage to V_{clamp}. The overvoltage clamp threshold is preset to 28 V if the V_{clamp} pin is left floating, otherwise it can be externally adjusted in the range of 10 to 52 V by connecting a resistor divider (R_1,R_2) of appropriate value between the V_{clamp} pin, V_{OUT} and GND.

The setting procedure is similar to that of UVLO, the internal divider current being fixed to 10 µA.

Given the desired V_{clamp} threshold, for a fixed value of the lower resistor R_2, **Equation 2** can be used to calculate the upper resistor R_1

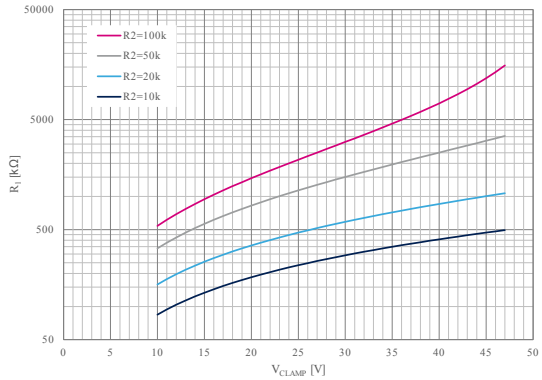
Equation 2

$$R_1 = \frac{1}{\frac{(1/R_2 + 10^{-2})}{(V_{clamp} - 1)} - \frac{1}{2700}}$$

(resistor values are expressed in kΩ)

Figure 8. Clamping voltage (V_{clamp}) vs. R_1, R_2 shows the relation between R_1 and the clamping voltage, for some fixed values of R_2.

Figure 8. Clamping voltage (V_{clamp}) vs. R_1, R_2



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5.1.4 Current limit

The STEF01 embeds an overcurrent sensing circuit, based on an internal N-channel Sense FET with a fixed ratio, used to monitor the output current (Figure 1. Block diagram).

The current limiting circuit responds to overcurrent events by reducing the conductivity of the power MOSFET, in order to clamp the output current at a safe value.

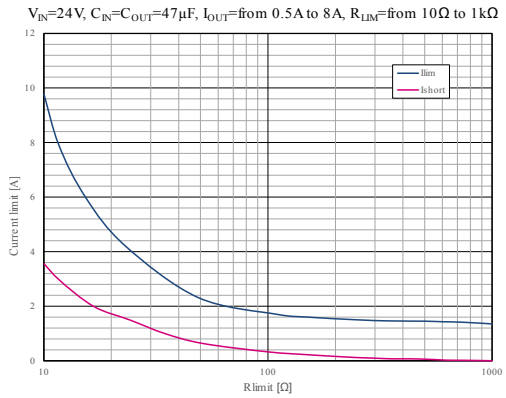
The overcurrent protection trip-point can be selected externally by means of the limiting resistor R_{Limit}, according to the graphs in Section 5.1.4 and Figure 28. Current limit vs. R_{limit} (zoom).

The circuit features two levels of current limitation, each one valid for a certain range of output voltage (V_{OUT}).

In case of overload, when the input current surpasses the programmed overload current limit (I_{LIM}), but the output voltage is still higher than 5.5 V (typ.), the device clamps the current to the I_{LIM} value.

If case of strong overload or short circuit, when the output voltage decreases to less than 3.5 V, the device enters the foldback current limit, with the current limited to a lower value (I_{SHORT}) that is typically 1.5 A when R_{Limit} = 22 Ω.

Figure 9. Current limit vs. R_{limit}



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During startup, the foldback current limit is disabled and the current is limited by the overcurrent protection at the I_{LIM} value. Please refer also to Section 5.4 Maximum load at startup for more details.

It is important to note that the R_{Limit} is mandatory for the current limiting circuit to function properly. It is recommended to use R_{Limit} value according to Table 3. Recommended operating condition and to the package power dissipation.

Important: very low values of R_{Limit} or failure to connect it may lead to malfunctioning of the current limiting circuit and to device damage.

5.2 Protection circuits

Since the power dissipation can reach remarkable levels during startup into heavy capacitive loads, large load transients and short-circuit during operation at high voltage, the STEF01 is protected by means of two circuits: the absolute thermal protection and the maximum power dissipation protection.

5.2.1 Thermal protection

The thermal protection is a standard thermal shutdown feature, which acts when the die temperature exceeds the absolute shutdown threshold, set typically to 175 °C.

The behavior of the STEF01 at thermal protection intervention can be changed by the user through the external Auto pin. This pin is internally pulled up.

When the Auto pin is left floating or connected to a voltage higher than 1 V, the thermal protection works as latched. If the device temperature exceeds the thermal shutdown threshold, the thermal shutdown circuitry turns the power MOSFET off, disconnecting the load. The EN/Fault pin of the device will be automatically set at an intermediate voltage, typically 1.4 V, in order to signal the overtemperature event.

The E-fuse can be reset either by cycling the supply voltage or by pulling down the EN pin below the V_{il} threshold and then releasing it.

When the AUTO pin is connected to GND or to a voltage lower than 0.4 V, the thermal protection works as auto-retry. Once the thermal protection threshold is reached, the power is turned off and remains in an off state until the die temperature drops below the hysteresis value. Once this occurs, the internal auto-retry circuit initiates a new startup cycle, with controlled dv/dt. During the shutdown period, the EN/Fault pin of the device will be automatically set to 0 V.

5.2.2 Maximum dissipated power protection

Besides the standard thermal shutdown described in Section 5.2.1 Thermal protection, which acts when the die temperature surpasses the absolute shutdown threshold, the STEF01 is equipped with advanced thermal protection, which limits the thermal power dissipated into the device. When the power dissipation is higher than the internal limit, the power transistor is turned off.

The power protection always acts in auto-retry mode, regardless of the Auto pin status. Its intervention is signaled on the EN/FAULT pin with a LOW logic state. If the fault persists, the die temperature may reach the thermal protection limit. If this happens, the device behavior is the one fixed by the user through the Auto pin signal.

The maximum dissipated power protection is able to protect the device from very fast overheating events, such as those caused by a short circuit on the output during operation.

5.3 Soft start function

The inrush current profile is controlled through a dedicated soft-start circuit. The startup time is set by default at 3 ms (typ.) and it can be prolonged by connecting a capacitor between the $C_{dv/dt}$ pin and GND. Figure 11. Startup time illustrates the turn-on sequence.

The turn-on time is defined as the time interval t_{ON} between assertion of the enable signal and the Vout reaching the ($V_{OUT(NOM)}$-2 V) voltage. The turn-on time is a function of the $C_{dv/dt}$ capacitor, the input voltage V_{CC} and the clamping voltage V_{Clamp}.

Given the $C_{dv/dt}$ external capacitor value, the turn-on time can be estimated using **Equation 3** and the graph in Figure 12. Startup time vs $C_{dV/dt}$, valid for normal operating conditions ($V_{CC} < V_{Clamp}$). In case the startup occurs with power supply voltage higher than the clamping voltage ($V_{CC} > V_{Clamp}$), the total startup time will be longer. The equation is meant as a theoretical aid in choosing the $C_{dv/dt}$ capacitor, and does not take into account the capacitor tolerance, temperature and process variations.

Equation 3

$$t_{ON} = 0.952 \cdot \frac{V_{CC}}{V_{Clamp}} \cdot \frac{(300 + C_{dvdt})}{113000} + t_{delay}$$

where time is expressed in [s] and the capacitor in [pF]; tdelay ~ 170 µs, is the initial delay time.

Figure 11. Startup time

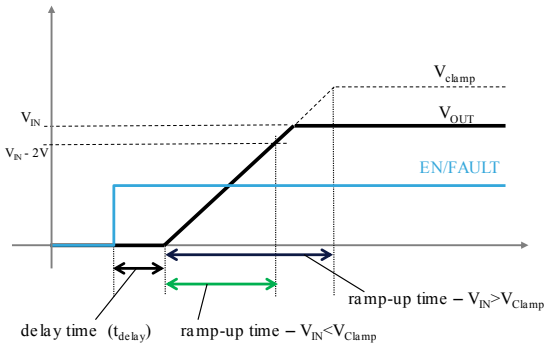

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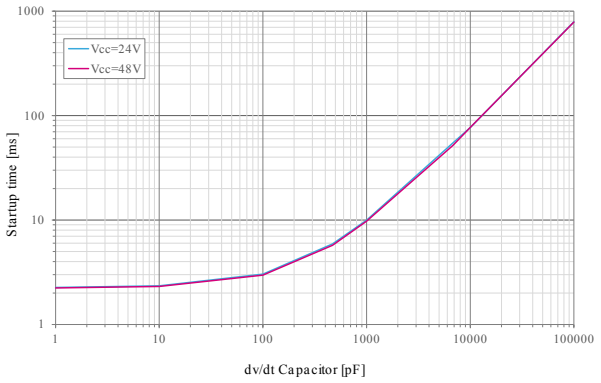
Figure 12. Startup time vs $C_{dV/dt}$



$C_{IN} = C_{OUT}$ = 22 µF, I_{OUT} = 0 mA, R_{LIM} = 11 Ω, V_{CLAMP} = 52 V for V_{CC} = 48 V, or V_{CLAMP} = 28 V for V_{CC} = 24 V

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5.4 Maximum load at startup

The power limiting function described in Section 5.2.2 Maximum dissipated power protection is designed to provide fast and effective protection for the internal FET.

Depending on supply voltage and load, it is possible that during startup the power dissipation is such that the maximum power protection is triggered and the output is shut down before the startup is complete. The EN/Fault signal is set according to Table 6. Enable/Fault pin behavior during thermal protection events.

In case of strong capacitive loads, the total startup time may be longer than the programmed startup time, since it is dependent also on the limitation current, the output load and the output capacitance value. In such a situation,

the foldback current limit could activate, so that the startup is longer or eventually interrupted by the intervention of thermal protection.

To avoid this occurrence, a longer startup time should be set by the appropriate selection of the $C_{dv/dt}$ capacitor.

5.5 Enable-fault pin

The Enable/Fault pin has the dual function of enabling/disabling the device and, at the same time, providing information about the device status to the application. The EN/Fault signal can be provided to a monitoring circuit to control the status of device.

It can be used as a standard Enable pin, (HI = enable, LO = disable) or connected to an external open-drain or open-collector device.

The EN/fault pin is internally pulled up to 5 V, therefore the device is enabled if the pin is left floating. In case of a thermal fault, the pin is pulled to an intermediate state, with a voltage of 1.4 V (typ.) (see Figure 6. UVLO threshold (V_{ON}) vs R_H, R_L).

The EN/Fault signal can be directly connected to the Enable/Fault pins of other STEF01 devices on the same application in order to implement a simultaneous enable/disable feature.

When a thermal fault occurs, the latch version can be reset either by cycling the supply voltage or by pulling down the Enable pin below the V_{il} threshold and then releasing it.

In the auto-retry operating mode, the power MOSFET remains in an off state until the die temperature drops below the hysteresis value. The EN/Fault pin is set to a low logic level and the auto-retry circuit attempts to restart the device with soft start.

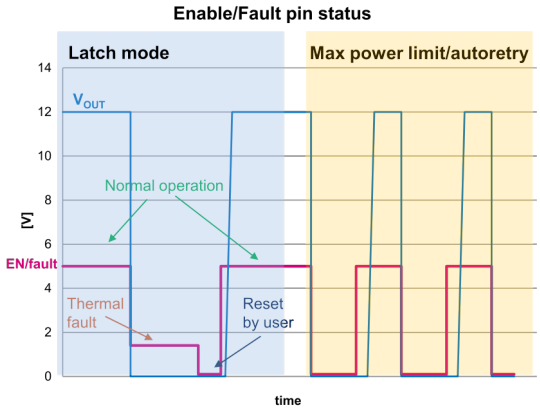
In case of power limit intervention, the EN/Fault pin is set to low logic level also. The following truth table and the graph in Figure 13. Enable/Fault pin status summarize the device behavior and the EN/Fault signal in all conditions.

Table 6. Enable/Fault pin behavior during thermal protection events

Auto pin logic level	Thermal protection status	Maximum power protection status	EN/Fault pin status	Output voltage
High	0	0	5 V	ON
High	1	X	1.4 V	OFF
High	0	1	0 V	OFF
Low	0	0	5 V	ON
Low	1	X	0 V	OFF
Low	0	1	0 V	OFF

Note: Maximum power protection always auto-retries (see Section 5.2.2 Maximum dissipated power protection).

Figure 13. **Enable/Fault pin status**



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5.6 Power Good function

Most applications require a flag showing that the output voltage is in the correct range. This function is achieved through the Power Good (PG) pin. The Power Good function on the STEF01 is accomplished by monitoring the voltage drop on the power pass element, $V_d = V_{CC}-V_{OUT}$.

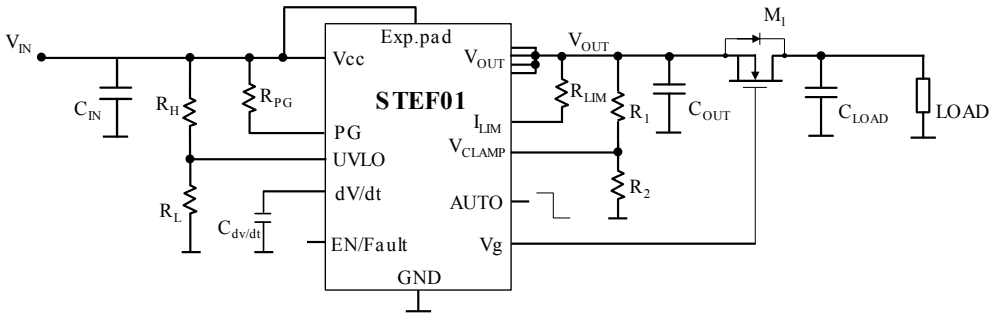
Whenever the V_D is lower than 1 V, the PG pin is in high impedance. If V_D is higher than 1 V, the PG pin goes to low impedance; therefore if either the device is functioning well or the EN pin is in low state, the PG pin is at high impedance.

The PG pin is an open drain pin, so it requires an external pull-up resistor, which must be connected between the PG pin and the desired high level voltage reference. The typical current capability of the PG pin is up to 6 mA. If the Power Good function is not used, the PG pin must remain floating.

5.7 Gate driver for reverse current blocking FET

Many applications require reverse current blocking (from load to input source) to permit the completion of important system activities or writing data to non-volatile memory prior to power down or during brownout. The STEF01 provides a V_g pin suitable to control an external blocking N-channel FET, connected back-to-back with the internal one, as shown in Figure 14. STEF01 with external reverse blocking FET.

Figure 14. **STEF01 with external reverse blocking FET**



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As V_{IN} drops during input power removal, the internal logic pulls the gate of the external MOSFET down, therefore both the internal pass element and the external MOSFET are turned off, blocking any current flow from the load to the power supply. In this case, the C_{LOAD} value is chosen according to the charge needed to complete the required operations.

The typical sourcing current of the Vg driver is 30 µA, with a voltage of 10 V compared to V_{OUT}. Therefore, when a low threshold MOSFET is used, the V_g must be clamped by means of a suitable external clamping diode.

When the EN pin is low, the external M1 FET is kept off by a 40 Ω internal pull-down so that the device is disabled by the user or by internal protection circuits.

5.8 External capacitors and application suggestions

Input and output capacitors are mandatory to guarantee device control loop stability and reduce the transient effects of stray inductances which may be present on the input and output power paths. In fact, when the STEF01 interrupts the current flow, input inductance generates a positive voltage spike on the input, and output inductance generates a negative voltage spike on the output. To reduce the effects of such transients, a C_{IN} capacitor of at least 10 µF must be connected between the input pin and GND, and located as close as possible to the device. For the same reason, a C_{OUT} capacitor of at least 47 µF must be connected at the output port.

In the event of a voltage clamp, with certain combinations of parasitic elements on the application, some small oscillations may be visible on the output voltage. This phenomenon does not affect device operation and can be mitigated by using an electrolytic capacitor for the C_{IN}.

When the device is powered via a power line made up of very long wires, where input inductance is higher than 3-4 µH, the input capacitor should be increased to 47 µF or more.

Additional protections and methods for addressing these transients are:

- Minimizing inductance of the input and output tracks
- TVS diodes on the input to absorb inductive spikes
- Schottky diode on the output to absorb negative spikes
- Combination of ceramic and electrolytic capacitors on the input and output

6 Typical performance characteristics

(The following plots are referred to the typical application circuit and, unless otherwise noted, at T_A = 25 °C)

Figure 15. Clamping voltage vs. temperature

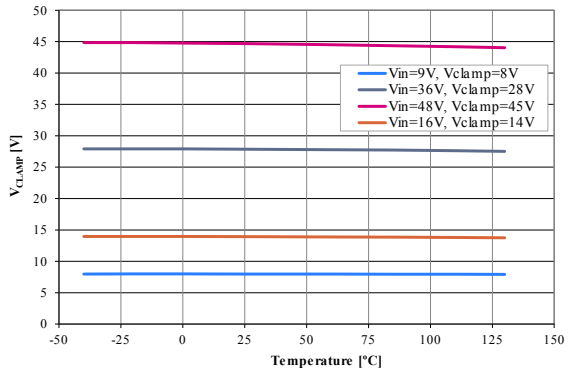

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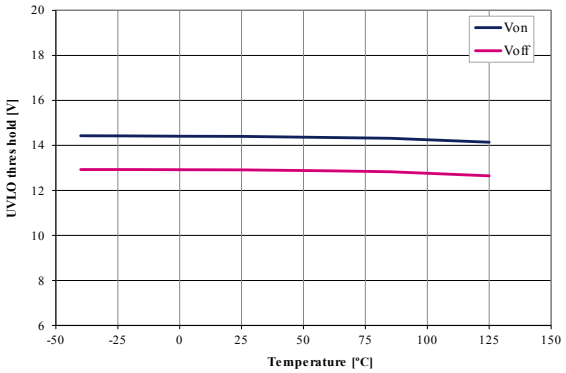
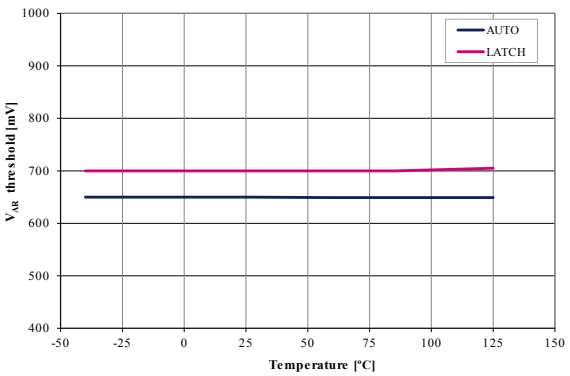
Figure 16. UVLO voltage vs. temperature



I_{OUT} = 10 mA,V_{IN} = from 10 V to 16 V, $V_{clampset}$ to 14 V

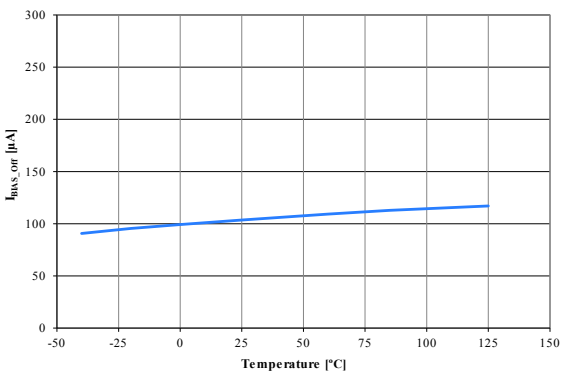
AMG180720171131MT

Figure 17. Auto pin thresholds vs. temperature



AMG180720171132MT

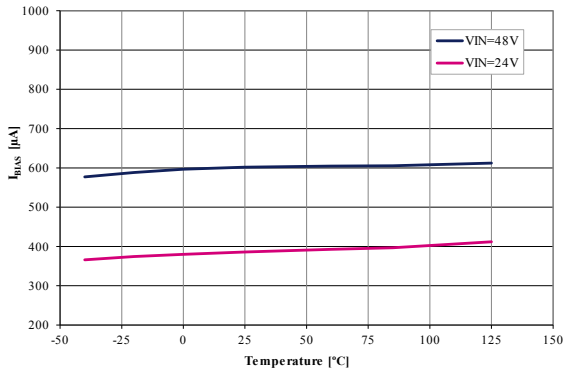
Figure 18. Off-state current vs. temperature



V_{IN} = 48 V , V_{EN} = GND

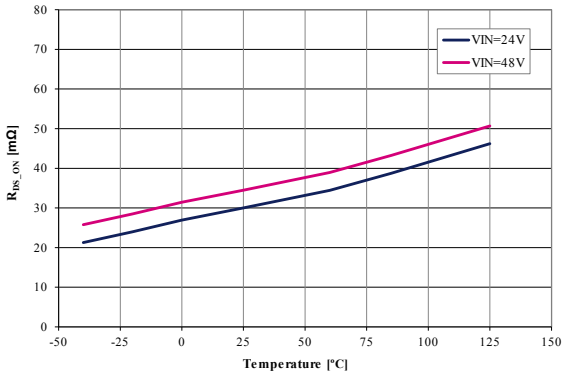
AMG180720171133MT

Figure 19. Bias current (device operational)



AMG180720171134MT

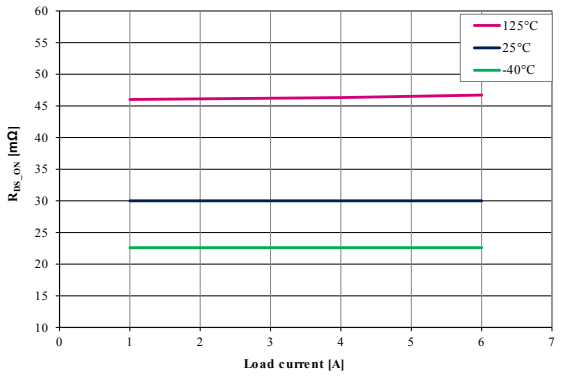
Figure 20. ON resistance vs. temperature



I_{OUT}= 1 A

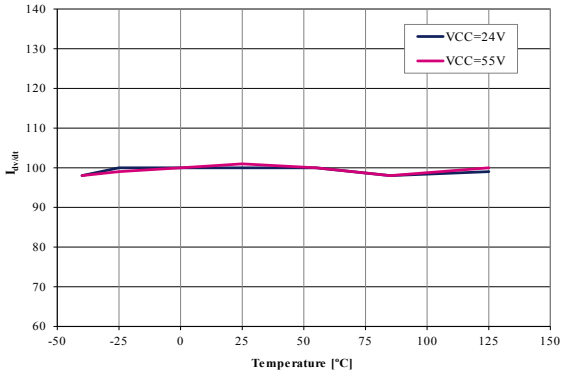
AMG180720171135MT

Figure 21. ON resistance vs. load current



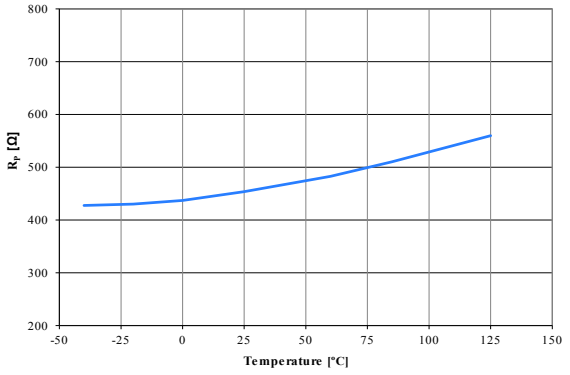
AMG180720171136MT

Figure 22. dv/dt pin current vs. temperature



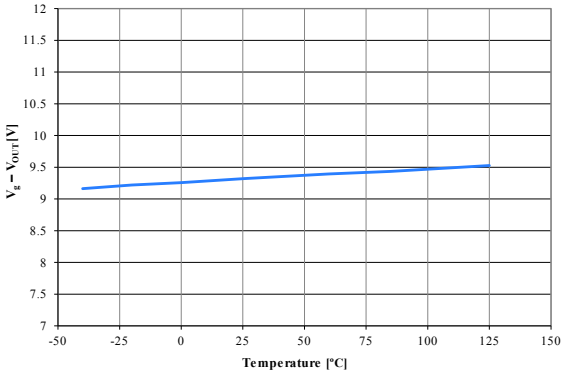
AMG180720171137MT

Figure 23. External gate driver pull-down resistance



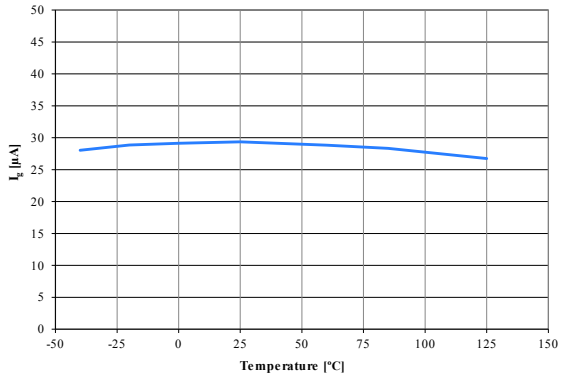
AMG180720171138MT

Figure 24. External gate driver voltage



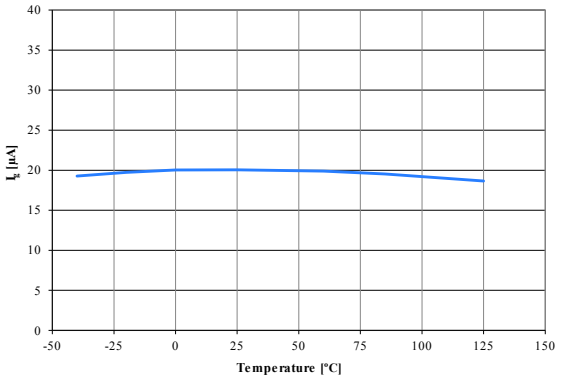
AMG180720171139MT

Figure 25. External gate driver current (source) vs. temperature



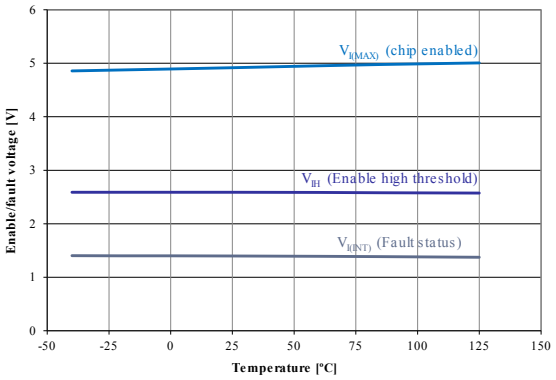
AMG180720171140MT

Figure 26. Low level En/Fault pin current (sink) vs. temperature



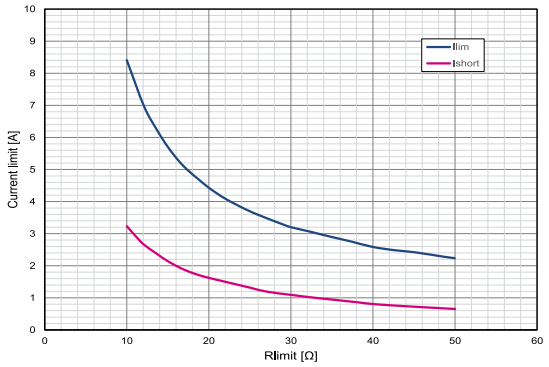
AMG180720171141MT

Figure 27. En/Fault pin voltage vs. temperature



AMG180720171142MT

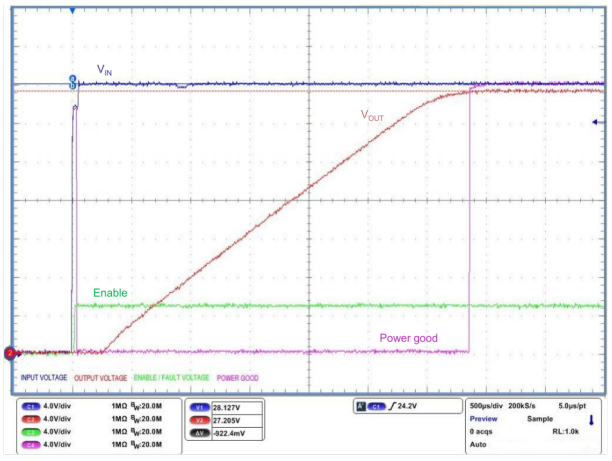
Figure 28. Current limit vs. R_{limit} (zoom)



V_{IN} = 24 V, C_{IN} = C_{OUT} = 47 µF, I_{OUT} = from 0.5 A to 8 A, R_{LIM} = from 10 Ω to 50 Ω

AMG180720171143MT

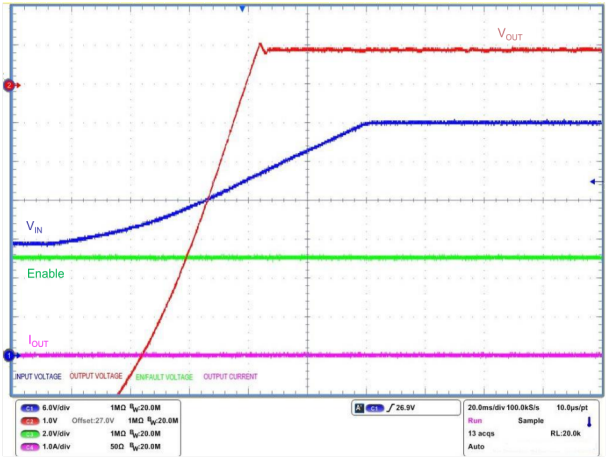
Figure 29. V_{OUT} ramp-up vs. Enable



V_{IN} = 28 V, C_{IN} = 22 µF, C_{OUT} = 22 µF, R_{LIM} = 11 Ω, V_{CLAMP} = 26 V, AUTO = GND

AMG180720171144MT

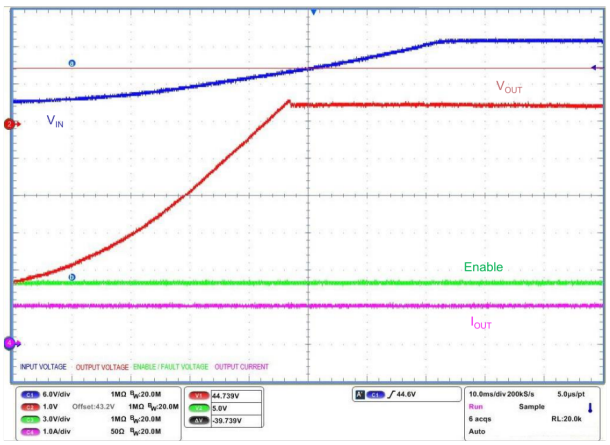
Figure 30. V_{OUT} clamping (28 V)



V_{IN} = from 20 V to 36 V, $V_{clampset}$ to 28 V, C_{IN} = 47 µF, C_{OUT} = 47 µF

AMG180720171145MT

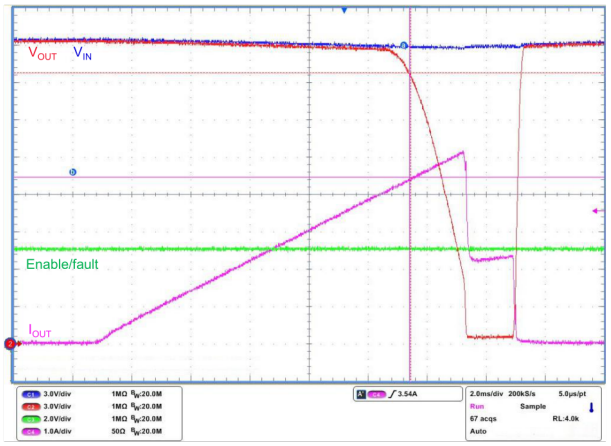
Figure 31. V_{OUT} clamping (44 V)



V_{IN} = from 36 V to 50 V, Vclampset to 44 V,
C_{IN} = 10 µF, C_{OUT} = 10 µF

AMG180720171146MT

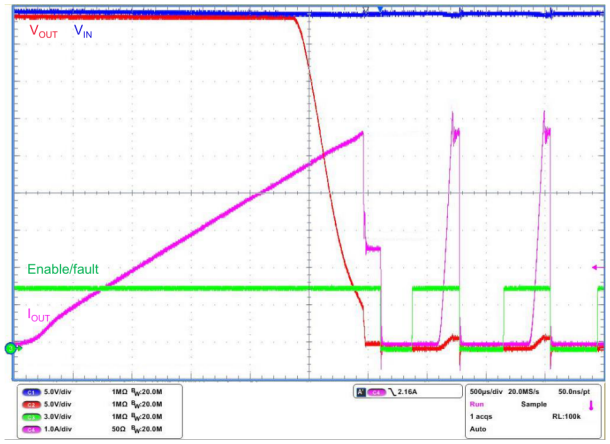
Figure 32. Response to overload (latch)



V_{IN} = 24 V, C_{IN} = C_{OUT} = 47 µF, I_{OUT} from 0 A to overload,
R_{LIMIT} = 22 Ω, AUTO = GND

AMG180720171147MT

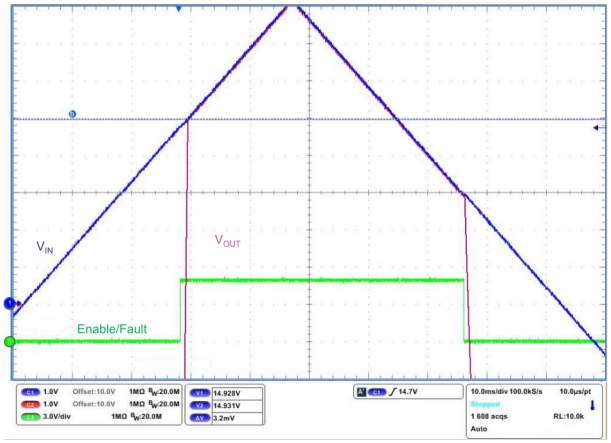
Figure 33. Response to overload (autoretry)



V_{IN} = 45 V C_{IN} = 47 µF, C_{OUT} = 1 µF, I_{OUT} from 0 mA to overload,
AUTO = FLOATING

AMG180720171148MT

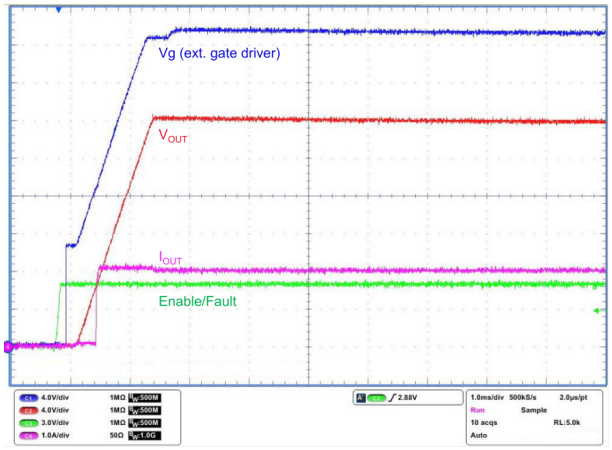
Figure 34. UVLO



V_{IN} = from 0 V to 20 V, C_{IN} = 22 µF, C_{OUT} = 22 µF, I_{OUT} = 10 mA, R_H,
R_L not connected

AMG180720171149MT

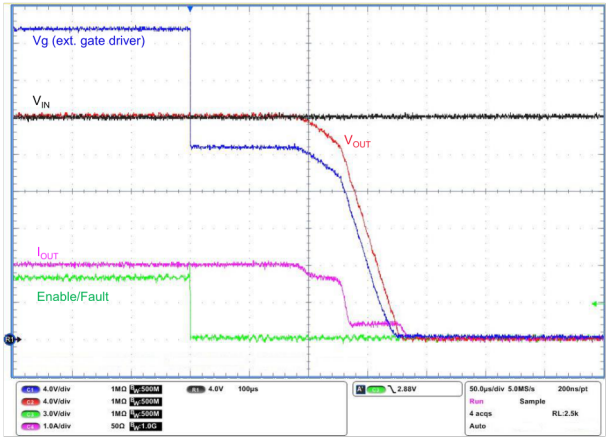
Figure 35. Enable turn-on with external FET



V_{IN} = 24 V, C_{IN} = 1 µF, C_{OUT} = 1 µF, R_{LIM} = 11 Ω, V_{CLAMP} = 50 V, I_{OUT} = 2 A, V_{OUT} measured after external FET

AMG180720171150MT

Figure 36. Enable turn-off with external FET



V_{IN} = 24 V, C_{IN} = 1 µF, C_{OUT} = 1 µF, R_{LIM} = 11 Ω, V_{CLAMP} = 50 V, I_{OUT} = 2 A, V_{OUT} measured after external FET

AMG180720171151MT

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

7.1 HTSSOP14 package information

Figure 37. HTSSOP14 package outline

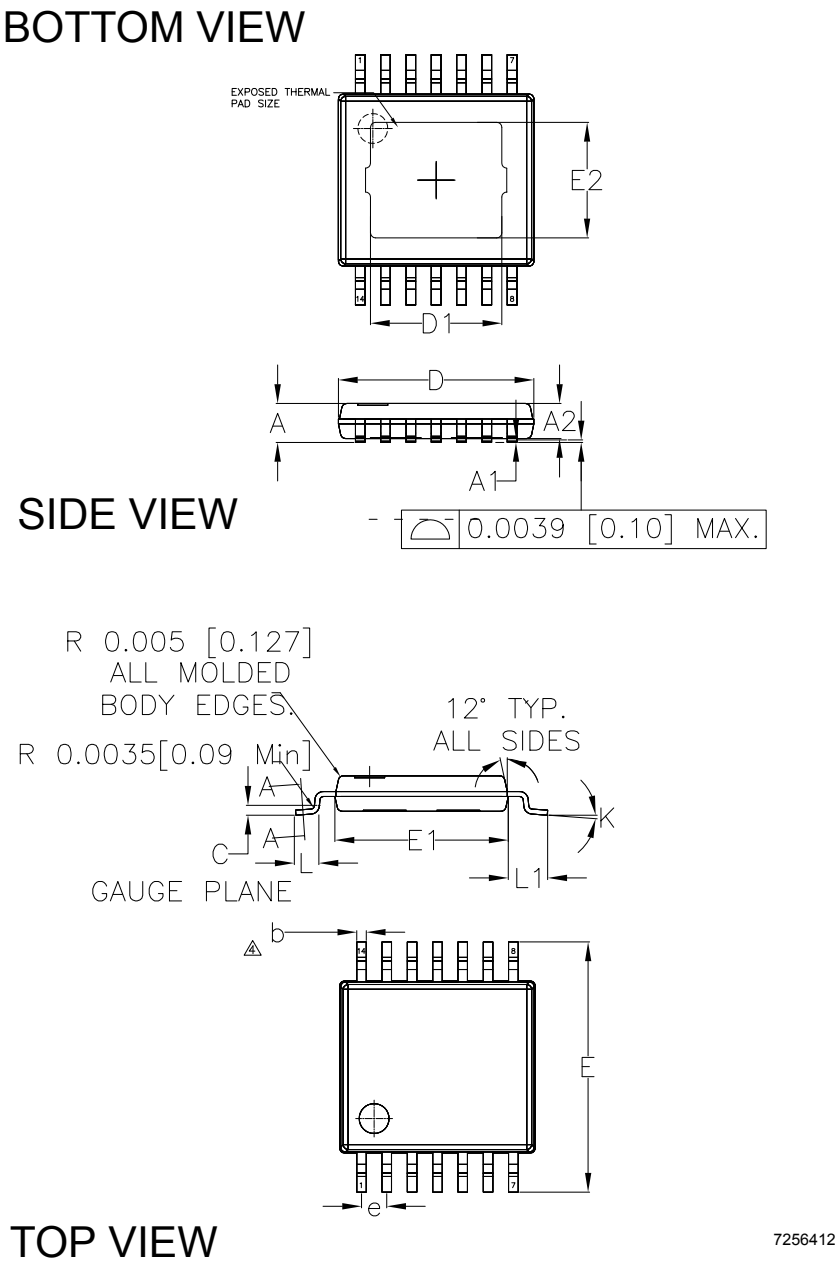
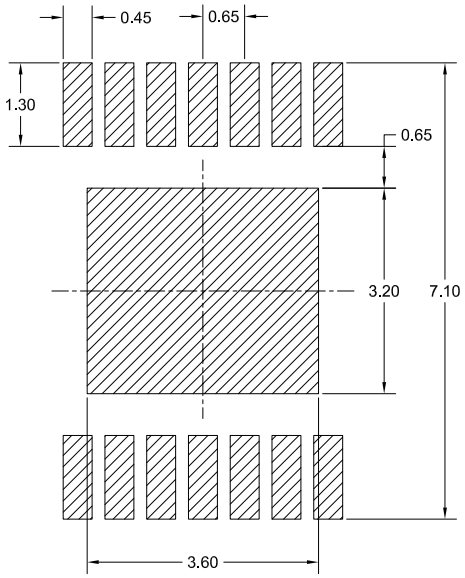


Table 7. HTSSOP14 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	1.00	1.10	1.20
A1	0.05	0.10	0.15
A2	0.80	1.00	1.05
b	0.19	0.25	0.30
c	0.09		0.25
D	4.90	5.00	5.10
D1	3.00		3.20
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
E2	3.00		3.20
e	0.65 BSC		
L	0.45	0.60	0.75
L1	0.95	1.00	1.05
k	0		8
aaa			0.10

Figure 38. HTSSOP14 recommended footprint



7.2 HTSSOP14 packing information

Figure 39. **HTSSOP14 carrier tape outline**

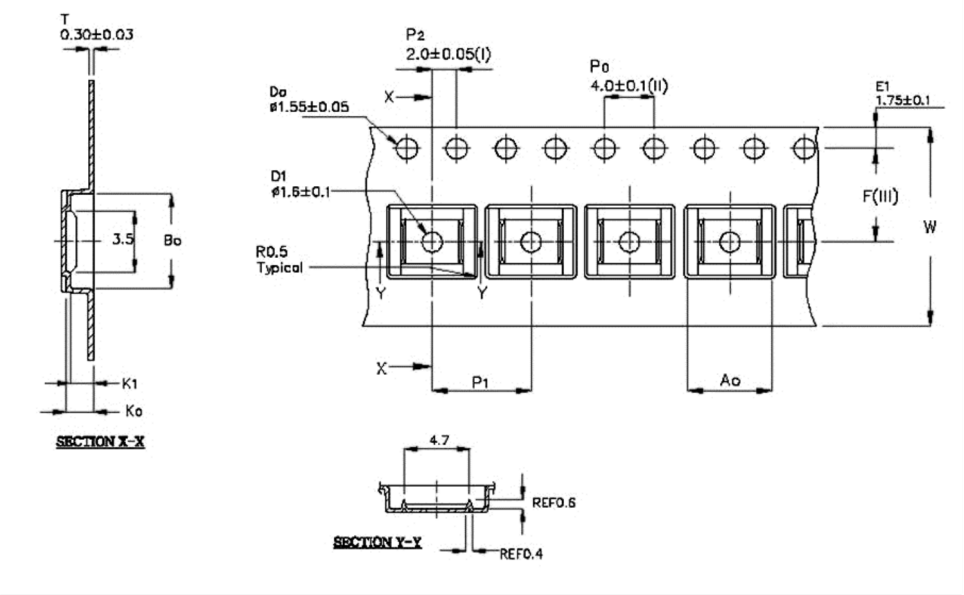


Table 8. **HTSSOP14 carrier tape mechanical data**

Dim.	Value (mm)
Ao	6.8 ±0.1
Bo	5.4 ±0.1
Ko	1.6 ±0.1
Ki	1.3 ±0.1
F	5.5 ±0.05
P1	8.0 ±0.1
W	12.0 ±0.3

Revision history

Table 9. **Document revision history**

Date	Revision	Changes
04-Aug-2017	1	Initial release.
15-Feb-2018	2	Update: I_D value Table 2. Absolute maximum ratings.
24-May-2018	3	Updated maturity status link on the cover page.
13-Jul-2018	4	Updated pin 11 note Table 1. Pin description.

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