

# NCP2823AGEVB, NCP2823BGEVB

## NCP2823 Series Evaluation Board User's Manual



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### EVAL BOARD USER'S MANUAL

#### Overview

The NCP2823A/B are cost effective mono audio power amplifiers designed for portable electronic devices. NCP2823A is optimized for 8  $\Omega$  operation and NCP2823B can operate with speaker impedance down to 4.0  $\Omega$ . For Instance, NCP2823B is capable of delivering 3 W of continuous average power to a 4.0  $\Omega$  from a 5.0 V supply in a Bridge Tied Load (BTL) configuration. Under the same conditions, NCP2823A can provide 1.5 W to an 8.0  $\Omega$  BTL load with less than 1% THD+N. For cellular handsets or

PDA's it offers space and cost savings because no output filter is required when using inductive transducers. With more than 95% efficiency and very low shutdown current, it increases the lifetime of your battery and drastically lowers the junction temperature.

The intent of the evaluation boards is to illustrate typical operation of the NCP2823 device for laboratory characterization. The NCP2823 Series Evaluation Board schematic is depicted in Figure 3.

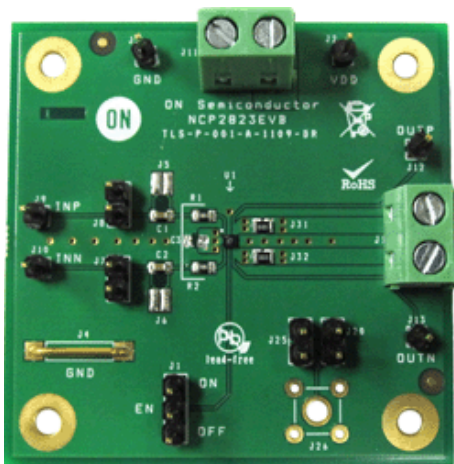


Figure 1. NCP2823AGEVB Board Picture

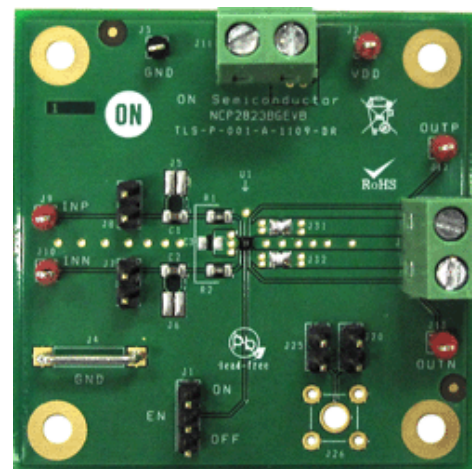


Figure 2. NCP2823BGEVB Board Picture

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## BOARD SCHEMATIC

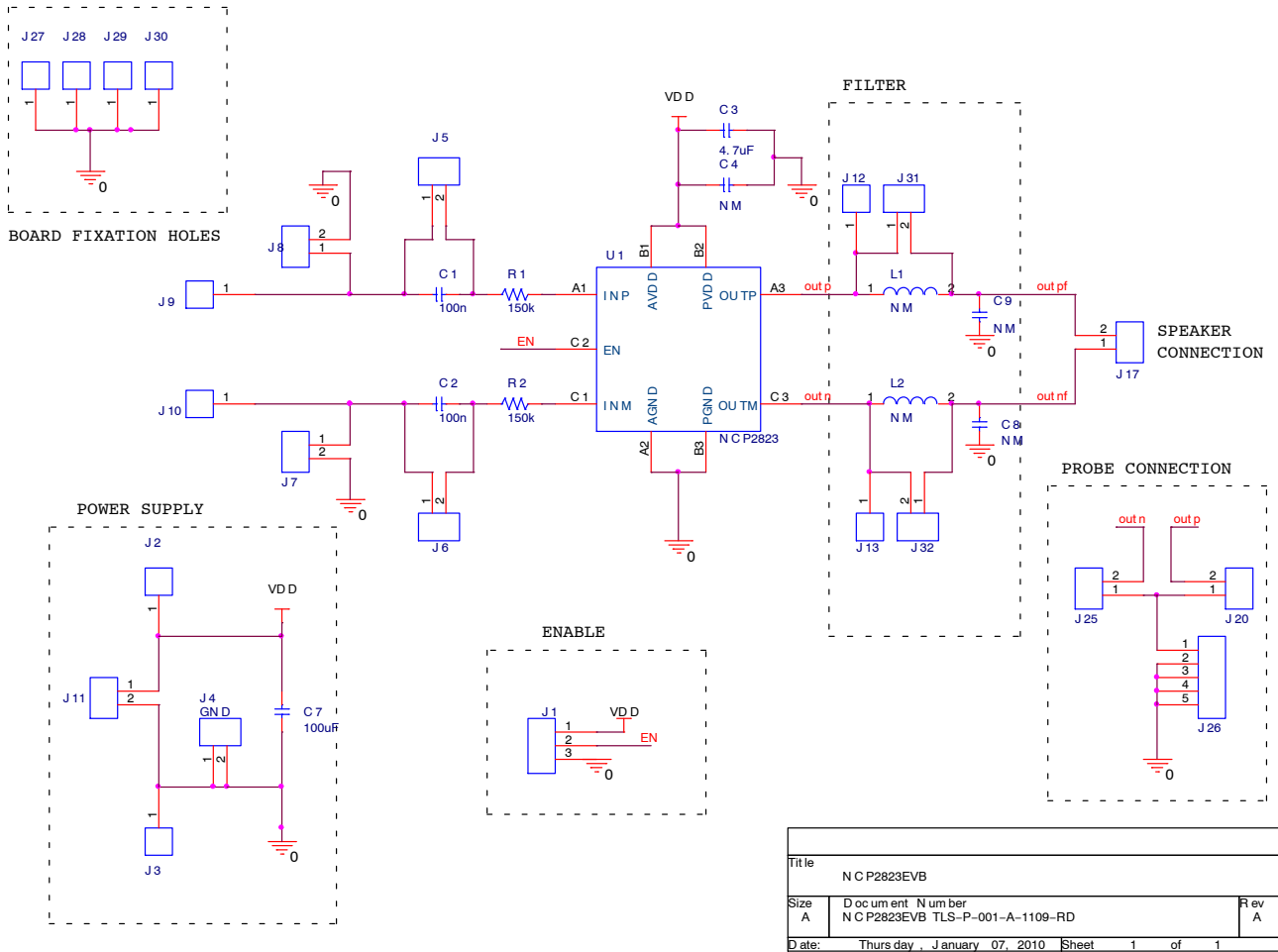


Figure 3. NCP2823 Series Evaluation Board Schematic

## OPERATION

The operating power supply of the NCP2823 is from 2.5 to 5.5 V. The absolute maximum input voltage is 7.0 V. A power supply set to 3.6 V and current limit set to at least 1.5 A must be connected to J11 connector to powering the NCP2823 Series Evaluation Board. Also to compensate for parasitic inductance of wires between the power supply and the evaluation board it is highly recommended to connect a 470  $\mu$ F electrolytic capacitor to bypass J11 terminal. Like this the device can be evaluate under powering condition very similar that battery power supplies.

### Performances of EVB Solution

To be as close as possible with final handset application, the design of this power conversion solution used small size footprints where possible. Changing components may positively or negatively impact the evaluation board performance, illustrated in Figure 4 to 9. For more information please refer to the NCP2823 datasheet.

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**Table 1. BOARD CONNECTIONS**

## INPUT POWER

| Symbol | Descriptions   |
|--------|--|
| J11-1  | This is the positive connection for power supply. The leads (positive + ground) to the input supply should be twisted and kept as short as possible. |
| J11-2  | This is the return connection for the power supply (Ground signal)   |
| J4     | Ground clip  |

## AUDIO

| Symbol | Descriptions          |
|--------|-----------------------|
| J9     | Positive Audio input  |
| J10    | Negative Audio input  |
| J17-2  | Positive Audio output |
| J17-1  | Negative Audio output |

## SWITCHES SETUP

| Symbol | Switch Descriptions                               |
|--------|---|
| J1     | Enable  |
| J5     | Short input capacitor on positive input           |
| J6     | Short input capacitor on negative input           |
| J7     | Connect the positive audio input to Gnd           |
| J8     | Connect the negative audio input to Gnd           |
| J31    | Short filter on positive output                   |
| J32    | Short filter on negative output                   |
| J25    | Connect negative output to Probe connection (J26) |
| J20    | Connect Positive output to Probe connection (J26) |

## TEST POINT

| Symbol | Switch Descriptions                                       |
|--------|---|
| J3     | This test point is directly connected to the GND          |
| J2     | This test point is directly connected to the Vdd pin      |
| J9     | This test point is connected to the positive audio input  |
| J10    | This test point is connected to the negative audio input  |
| J12    | This test point is connected to the positive audio output |
| J13    | This test point is connected to the negative audio output |
| J26    | Probe connection  |

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## TYPICAL OPERATING CHARACTERISTICS

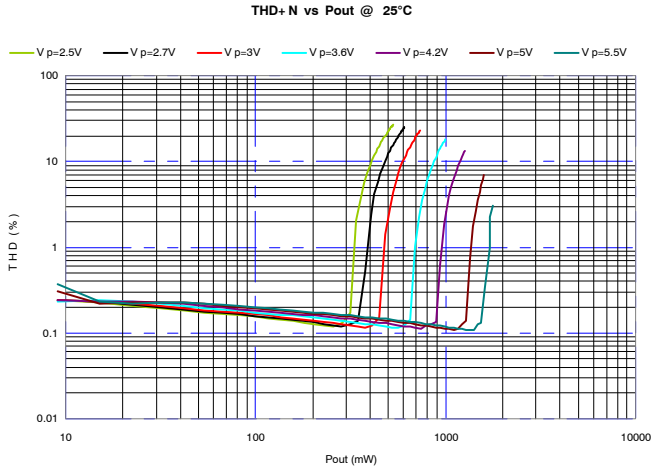


Figure 4. THD vs.  $P_{OUT}$ ,  $R_I = 8 \Omega$ ,  $f = 1 \text{ kHz}$

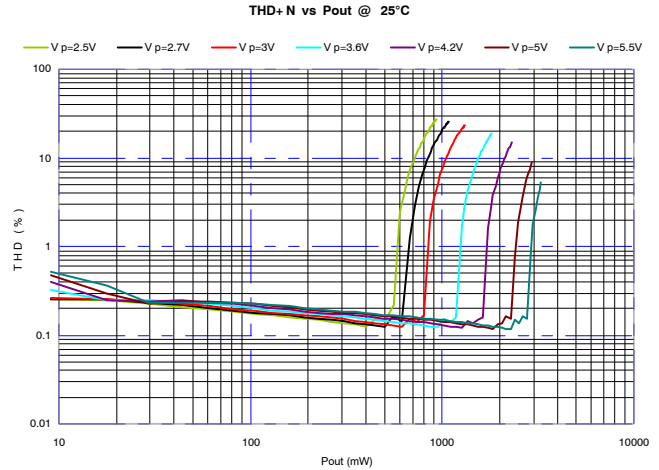


Figure 5. THD vs.  $P_{OUT}$ ,  $R_I = 4 \Omega$ ,  $f = 1 \text{ kHz}$

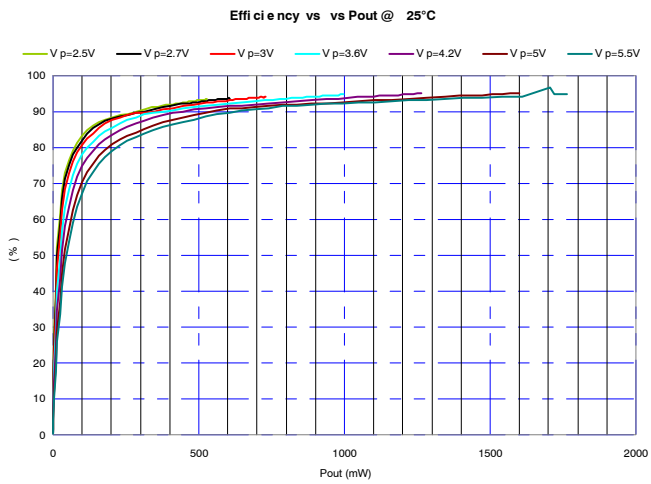


Figure 6. Efficiency vs.  $P_{OUT}$ ,  $R_I = 8 \Omega$ ,  $f = 1 \text{ kHz}$

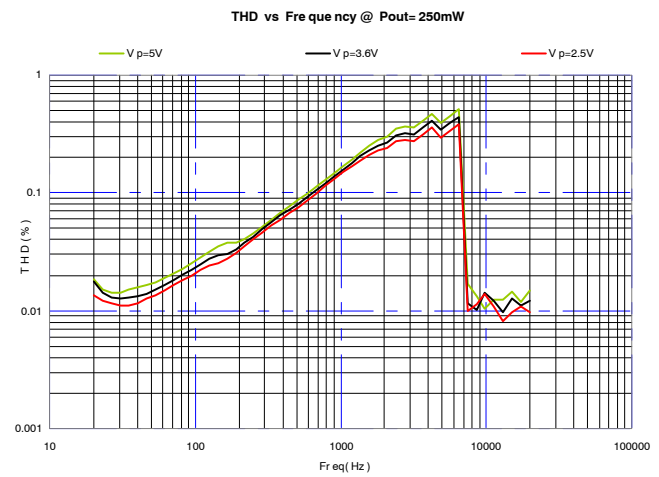


Figure 7. THD vs. Frequency,  $R_I = 8 \Omega$ ,  $P_{OUT} = 250 \text{ mW}$

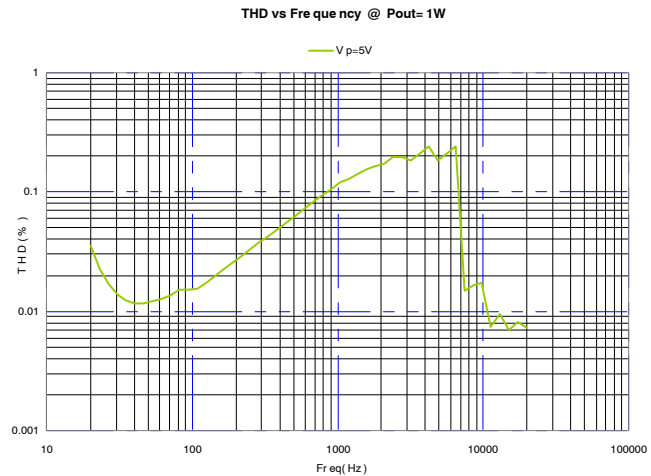


Figure 8. THD vs. Frequency,  $R_I = 8 \Omega$ ,  $P_{OUT} = 1 \text{ W}$

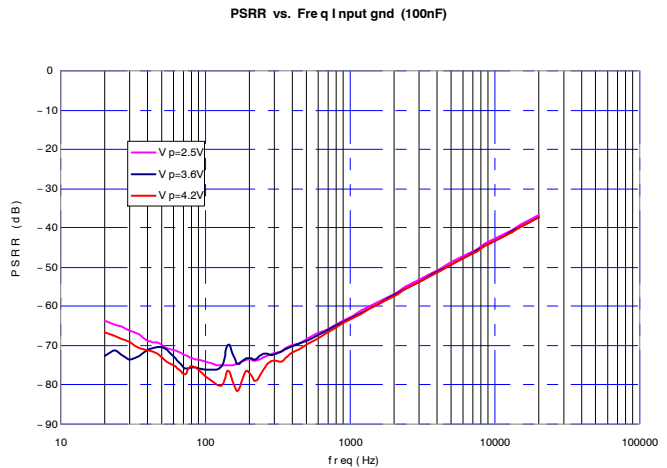


Figure 9. PSRR vs. Frequency

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## PCB LAYOUT

As with all Class D amplifier, care must have been observed to place the components on the PCB and layout the critical nodes. The evaluation board is made of 4 PCB layers where first internal layer is a GND. Figure 10, Figure 12 and

Figure 13 show the layout of the NCP2823 Series evaluation board. For more specific layout guidelines please refer to the NCP2823 datasheet.

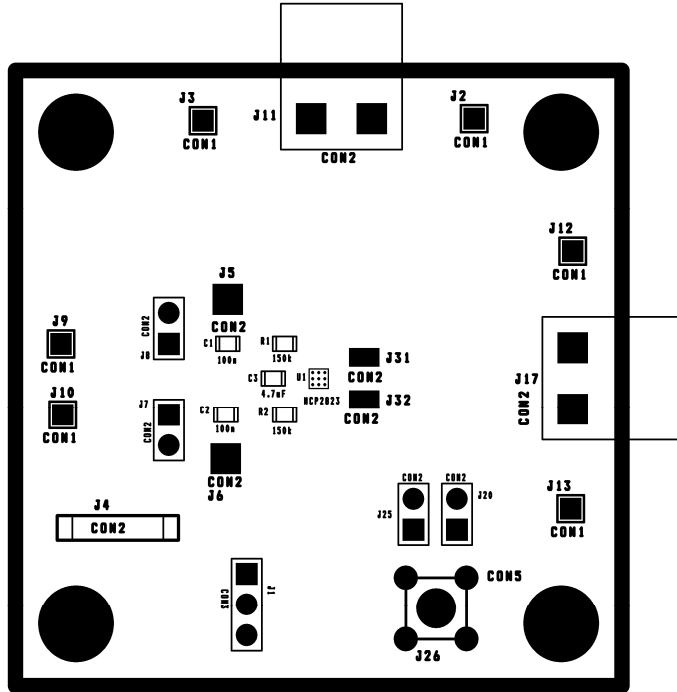


Figure 10. Assembly Layer TOP

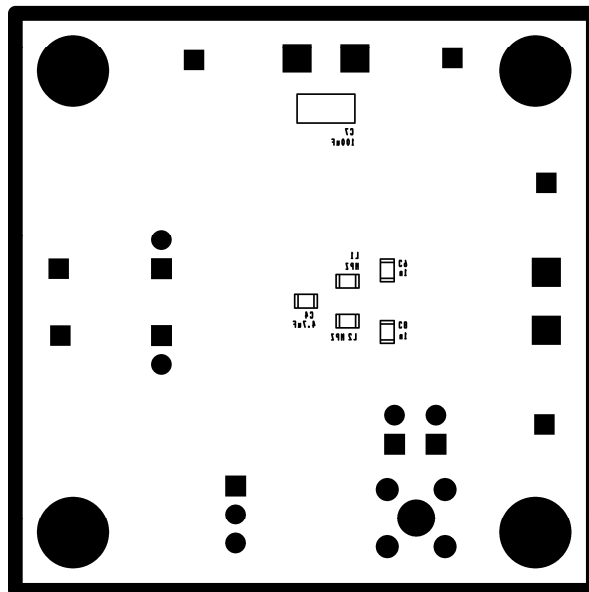


Figure 11. Assembly Layer BOTTOM

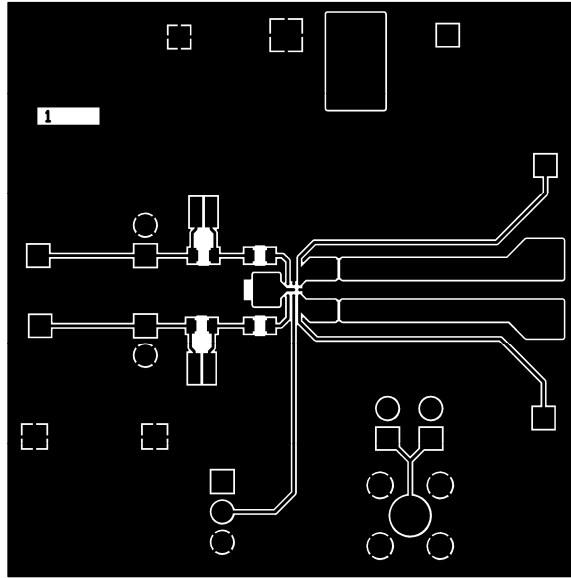


Figure 12. Top Layer Routing

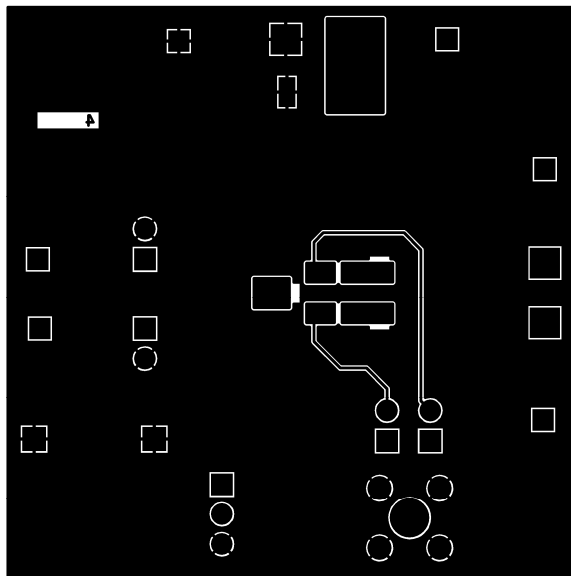


Figure 13. Bottom Layer Routing

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**Table 2. BILL OF MATERIALS**

| Qty | Ref Des.                     | Description                               | Size                       | Manufacturer     | Part Number                 |
|-----|------------------------------|---|----------------------------|------------------|-----------------------------|
| 1   | U1                           | NCP2823                                   | CSP-9<br>1.45 x 1.45<br>mm | ON Semiconductor | NCP2823                     |
| 2   | C1, C2                       | Capacitor, Ceramic 100 nF                 | 0603                       | KEMET            | C0603C104K5RAC              |
| 2   | C4                           | Capacitor, Ceramic 4.7 $\mu$ F 6.3 V      | 0603                       | KEMET            | C0603C475K9PAC              |
| 2   | R1, R2                       | Resistor 150k 1%                          | 0603                       | Std              | Any supplier possible       |
| 2   | J11,<br>J17                  | Mal. SL5.08/2/90B plus Fem. BLZ<br>5.08/2 |                            | Weidmuller       | SL5.08/2/90 +<br>BLZ 5.08/2 |
| 3   | J1                           | Header 3 pin, 100 mil spacing             | 0.100 x 2                  | Std              | Std                         |
| 2   | J7, J8                       | Header 2 pin, 100 mil spacing             | 0.100 x 2                  | Std              | Std                         |
| 1   | J7                           | GND Connection                            |                            | Std              | Std                         |
| 9   | J2, J3, J9,<br>J10, J12, J13 | Test Point                                |                            | Std              | Std                         |
| 2   | J31, J32                     | Soldering point must be connected         |                            |                  |                             |
| 1   | PCB                          | PCB 2.0 in x 2.0 in x 1.0 mm, 4 Layers    |                            | Any              | TLS-P-001-A-1109-RD         |

NOTE: Component J20, J25, J26, L1, L2, C8 and C9 are not mounted on this demokit.

## ASSEMBLY TEST PROCEDURE

A power supply set to 3.6 V and current limit set to at least 1.5 A must be connected to J15 connector to powering the NCP2823 Series evaluation board. Also to compensate for parasitic inductance of wires between the power supply and the evaluation board it is highly recommended to connect a 470  $\mu$ F electrolytic capacitor to bypass J11 terminal. Like this the device can be evaluate under powering condition very similar that battery power supplies.

These tests are provided in order to guarantee a good assembly of the NCP2823 on its dedicated board, it do not consist in parametric test which is already done at chip level.

### SHUTDOWN TEST

Switches setup for shutdown test:

| Symbol | Switch Description                     |
|--------|--|
| J1     | Must be connected to ground (low side) |

\*All other switches must be kept floating

Tests:

1. Set the switches in the configuration
2. Power the board with a 3.6 V power supply limited at 1.5A and bypassed by a 470  $\mu$ F electrolytic capacitor.
3. Measure the current on the power supply (must be inferior to 1  $\mu$ A)

### Wake up test

Switches setup for wire mode test:

| Symbol | Switch Description                   |
|--------|--------------------------------------|
| J1     | Must be connected to VDD (high side) |

\*All other switches must be kept floating

Tests:

4. Set the switches in the configuration
5. Power the board with a 3.6 V power supply limited at 1.5 A and bypassed by a 470  $\mu$ F electrolytic capacitor.
6. Measure DC Output voltage on J12 on J13 and GND. DC Voltage must be equal to 1.8 V
7. Measure DC input voltage on J5-2 on J6-2 and GND. DC Voltage must be equal to 1.26 V

### SUMMARY

| Test          | Measurement               | Switch Description          |
|---------------|---------------------------|-----------------------------|
| Shutdown test | I Supply                  | I < 1 $\mu$ A               |
| Wake up test  | VOUTP, VOUTN<br>VJ9, VJ10 | VDC = 1.8 V<br>VDC = 1.26 V |

NOTE: For each board a Test Result Table must be fully completed (see the next page)

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## TEST RESULT TABLE

| NCP2823 Assembly Test |                    |               |       |  |
|-----------------------|--------------------|---------------|-------|--|
| Date                  |                    | Operator Name |       |  |
| Board Serial Number   |                    |               |       |  |
| Test No.              | Test Name          | Results       | Value |  |
| 1                     | Shutdown mode test | I Supply      |       |  |
| 2                     | Wake up test       | VoutP, VoutN  | 1.8   |  |
|                       |                    | VJ9, VJ10     | 1.26  |  |

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