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Setting Up the Evaluation Board for the ADCLK905/ADCLK907/ADCLK925

PACKAGE LIST

Evaluation board with component installed
Applicable documents (schematic, layout, and so on)

GENERAL DESCRIPTION

This user guide describes how to set up and use the evaluation board for the ADCLK905/ADCLK907/ADCLK925. The same printed circuit board (PCB) is used to evaluate all three devices. The ADCLK905/ADCLK907/ADCLK925 data sheet should be used in conjunction with this user guide.

The data sheet contains full technical details about the specifications and operation of these devices.

The ADCLK905/ADCLK907/ADCLK925 clock buffers are very fast, making it important to use adequate high bandwidth instruments to evaluate them. To that end, the evaluation board is fabricated using a high quality dielectric material between layers to maintain high signal integrity. Transmission line paths are kept as close to 50 Ω as possible.

DIGITAL PICTURE OF THE EVALUATION BOARD

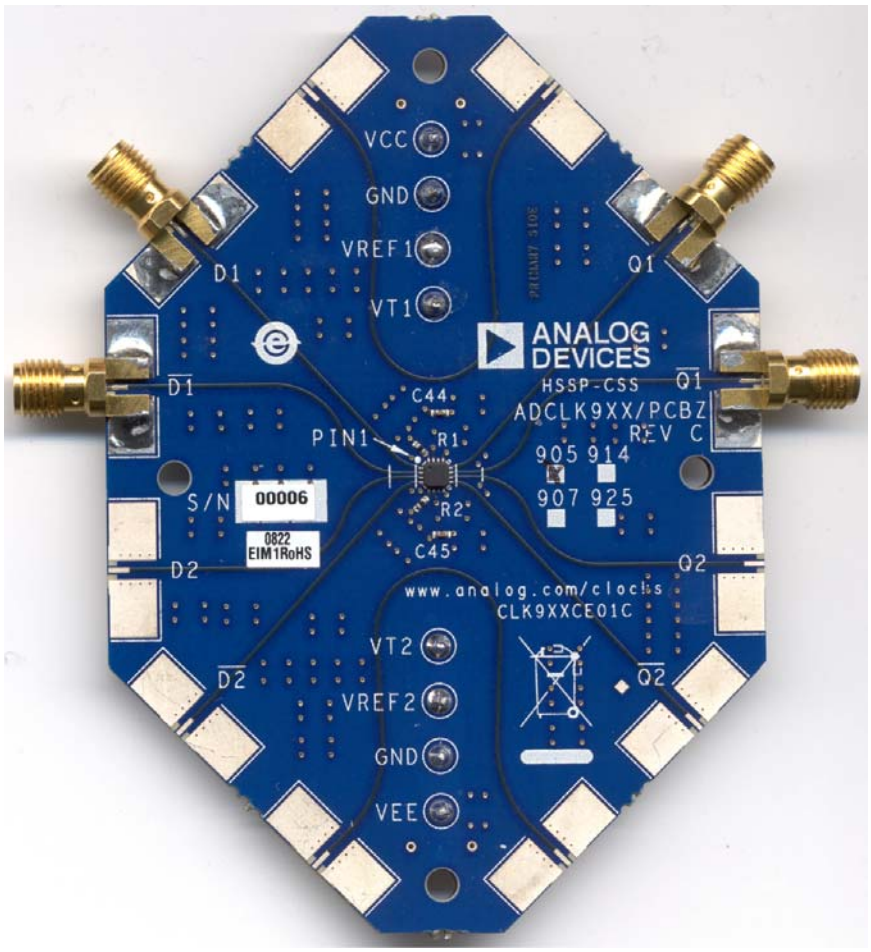

Figure 1. ADCLK905/ADCLK907/ADCLK925 Evaluation Board

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REVISION HISTORY

9/09—Revision 0: Initial Version

RECOMMENDED BOARD SETUP

The recommended setup for the evaluation board is shown in Figure 2. Note that there is no LVPECL output termination on the evaluation board. LVPECL termination is accomplished via the 50 Ω input of the oscilloscope. To meet the standard LVPECL output termination (V_{CC} − 2 V into 50 Ω), V_{CC} is set to 2 V and V_{EE} is set to −1.3 V. This also meets the requirement for $V_{CC} - V_{EE}$ = 3.3 V.

Table 1. Basic Equipment Required

Quantity	Description
1	Dual power supply
1	Signal source
1	High bandwidth oscilloscope
4	Matched high speed cables

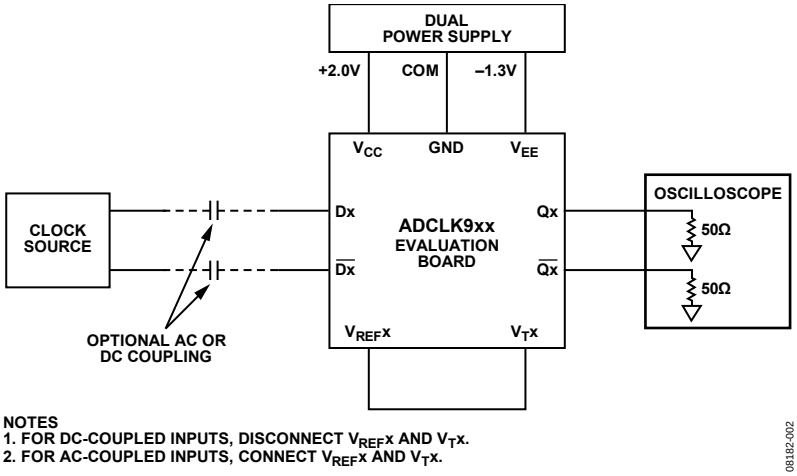

Figure 2. Recommended Setup for Device Evaluation

CLOCK INPUT CONFIGURATION

The clock inputs of the ADCLK905/ADCLK907/ADCLK925 on the evaluation board are dc-coupled to the SMA connectors. Therefore, the user must ac-couple the clock source, or the clock source must supply the appropriate dc common-mode voltage with adequate input swing.

It is recommended that the clock source be ac-coupled and that $V_{REF}x$ and $V_{T}x$ be tied together. For single-ended operation, ac-couple the unused input to ground with a 0.1 µF capacitor. For more information about input configurations, refer to the data sheet for the ADCLK905/ADCLK907/ADCLK925. Figure 3 to Figure 5 show block diagrams for the three devices.

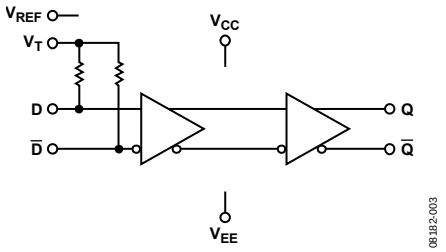

Figure 3. ADCLK905 1:1 Clock/Data Buffer

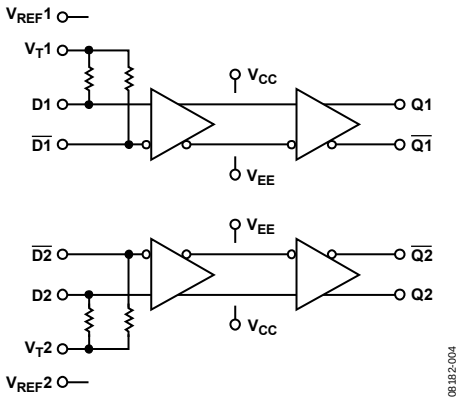

Figure 4. ADCLK907 Dual 1:1 Clock/Data Buffer

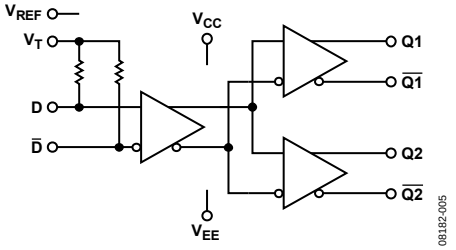

Figure 5. ADCLK925 1:2 Clock/Data Fanout Buffer

Table 2. Jumper Connections

Jumper	ADCLK905/ADCLK925	ADCLK907
TP1 (GND)	Connect to GND	Connect to GND
TP2 (VCC)	Connect to 2.0 V	Connect to 2.0 V
TP3 (VEE)	Connect to −1.3 V	Connect to −1.3 V
TP4 (GND)	Connect to GND	Connect to GND
TP5 (VREF1)	Short T5 and T6 for input ac coupling, else no connection	Short T5 and T6 for input ac coupling, else no connection
TP6 (VT1)	Short T5 and T6 for input ac coupling, else no connection	Short T5 and T6 for input ac coupling, else no connection
TP7 (VT2)	No connection	Short T7 and T8 for input ac coupling, else no connection
TP8 (VREF2)	No connection	Short T7 and T8 for input ac coupling, else no connection

EVALUATION BOARD SCHEMATICS AND ARTWORK

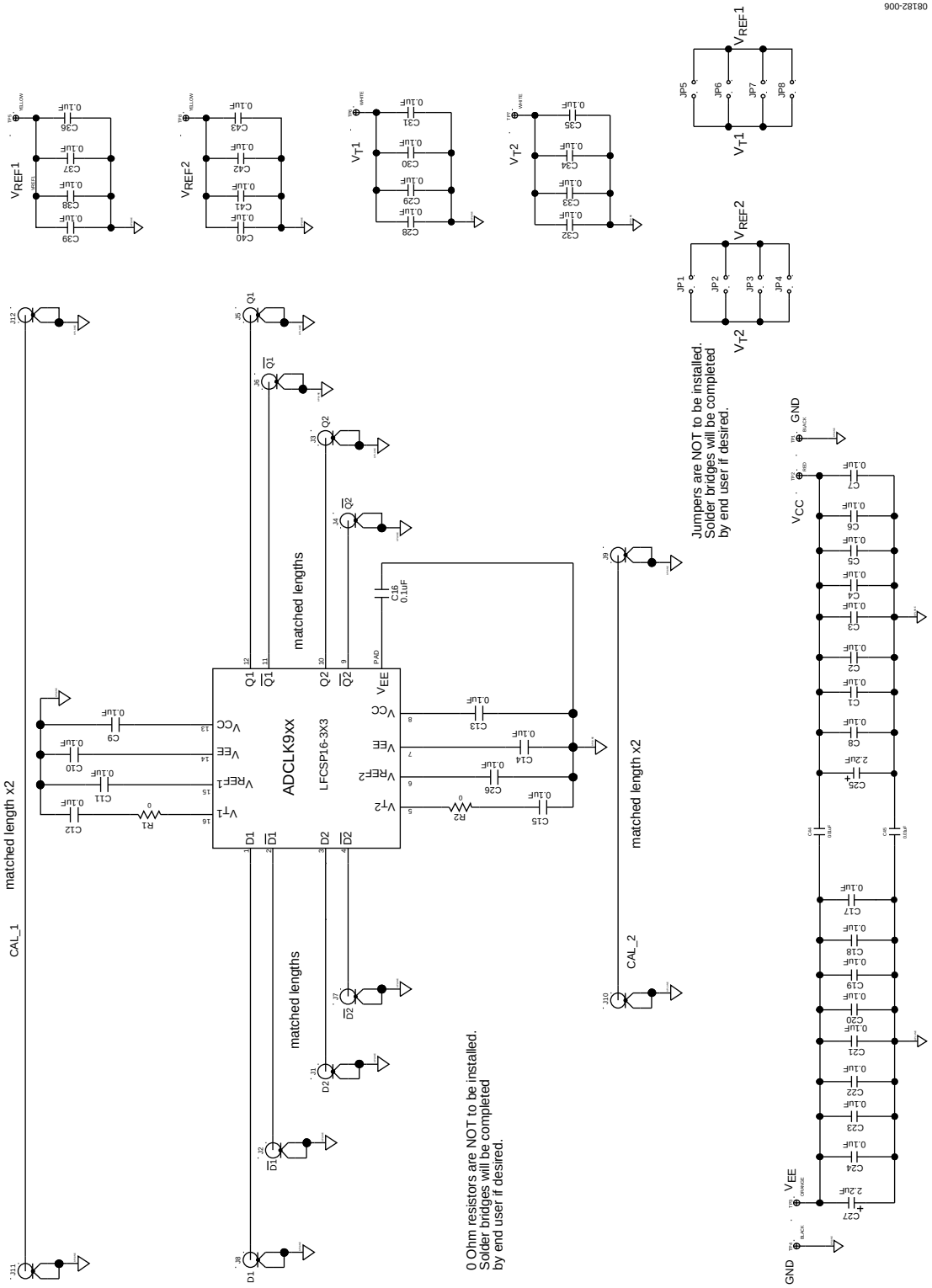

Figure 6. ADCLK905/ADCLK907/ADCLK925 Evaluation Board Schematic

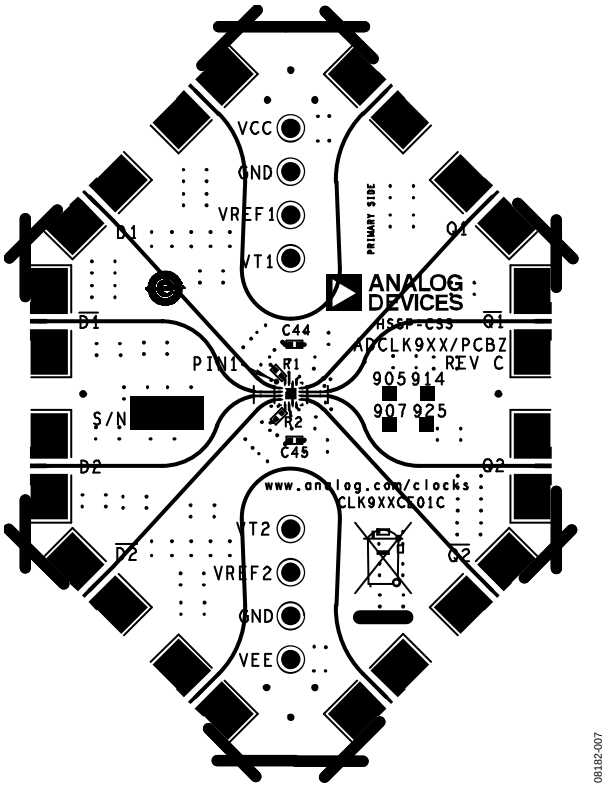

Figure 7. Top Trace Layer

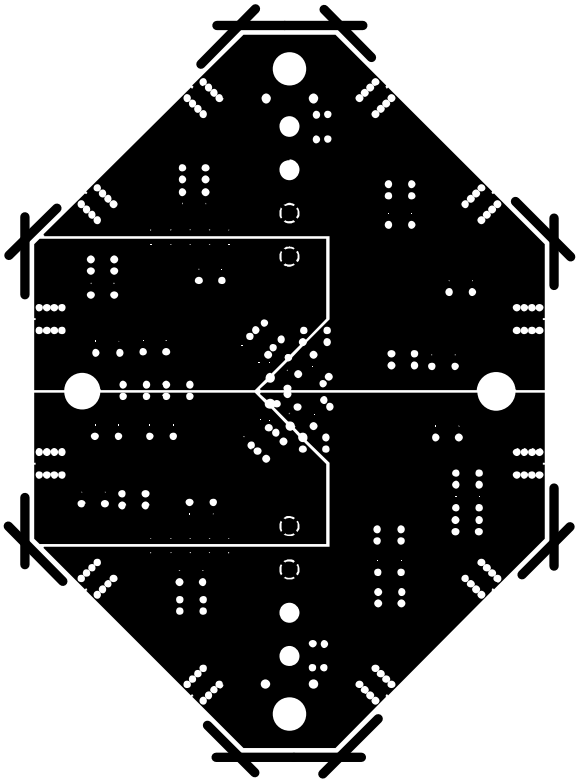

Figure 9. V_{REF} and V_T Plane Layers

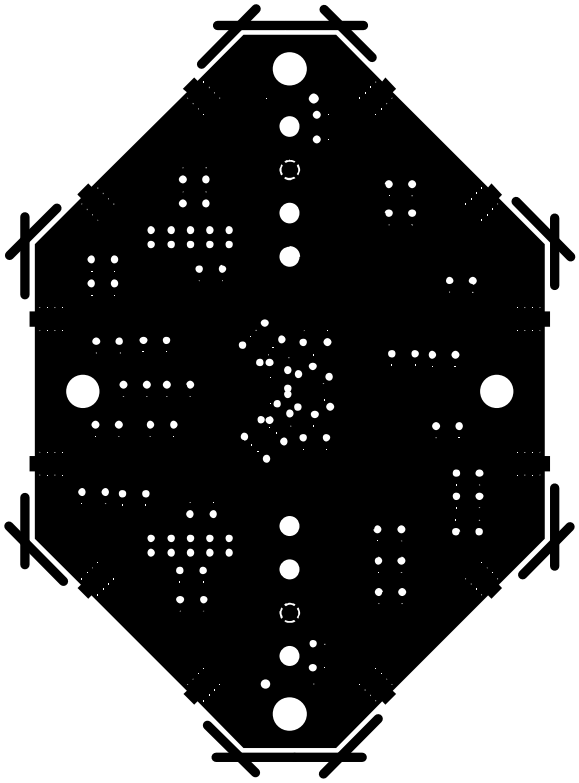

Figure 8. Ground Plane Layer

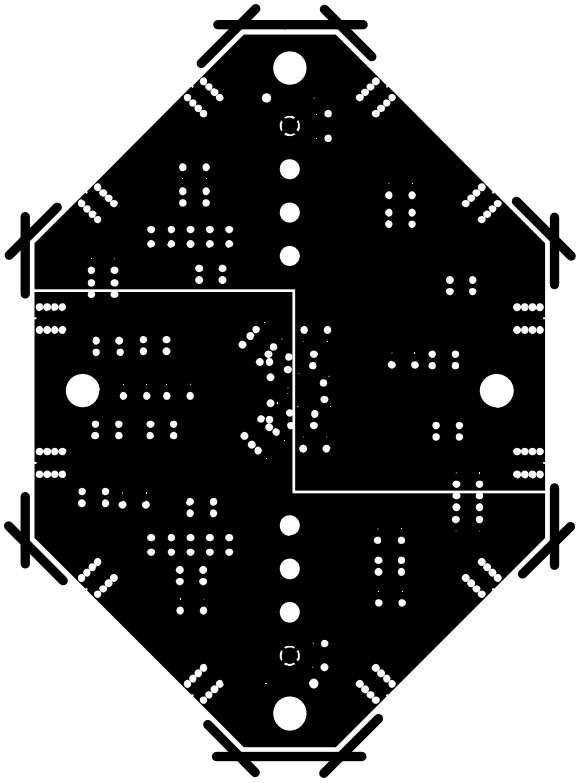

Figure 10. V_{CC} and V_{EE} Power Plane Layer

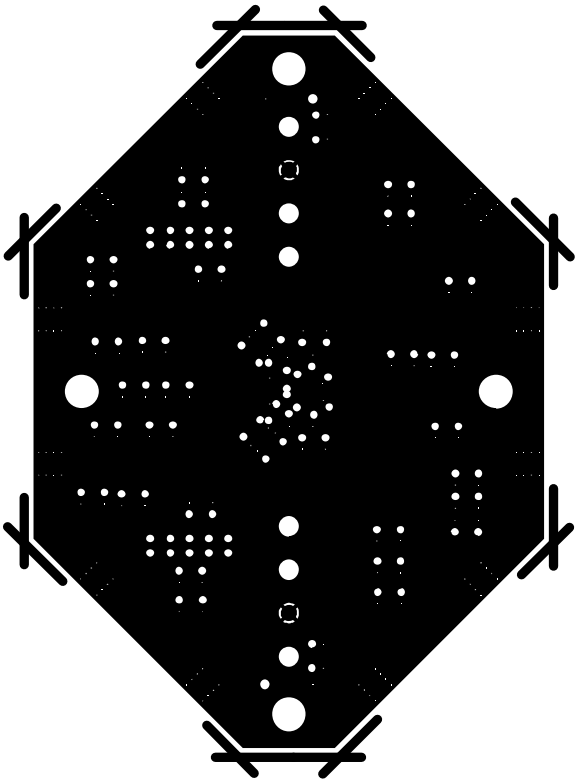

Figure 11. Second Ground Plane Layer

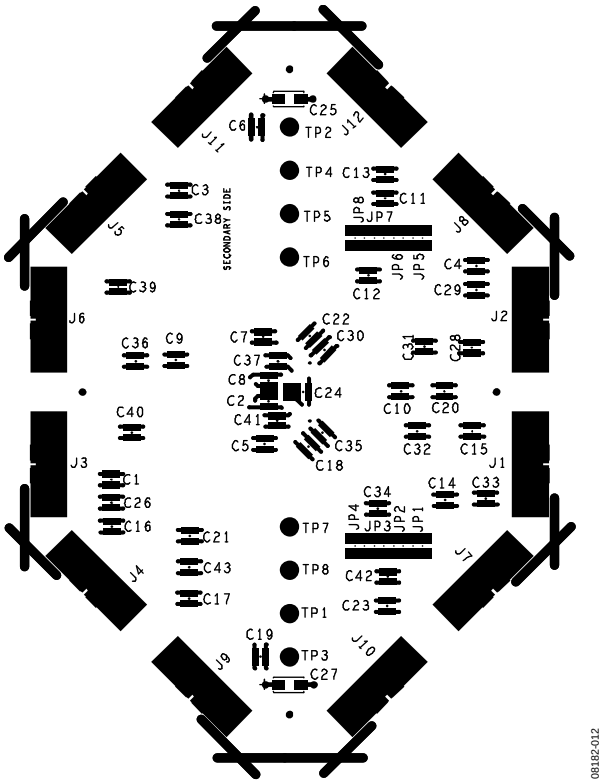

Figure 12. Bottom Trace Layer

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

NOTES