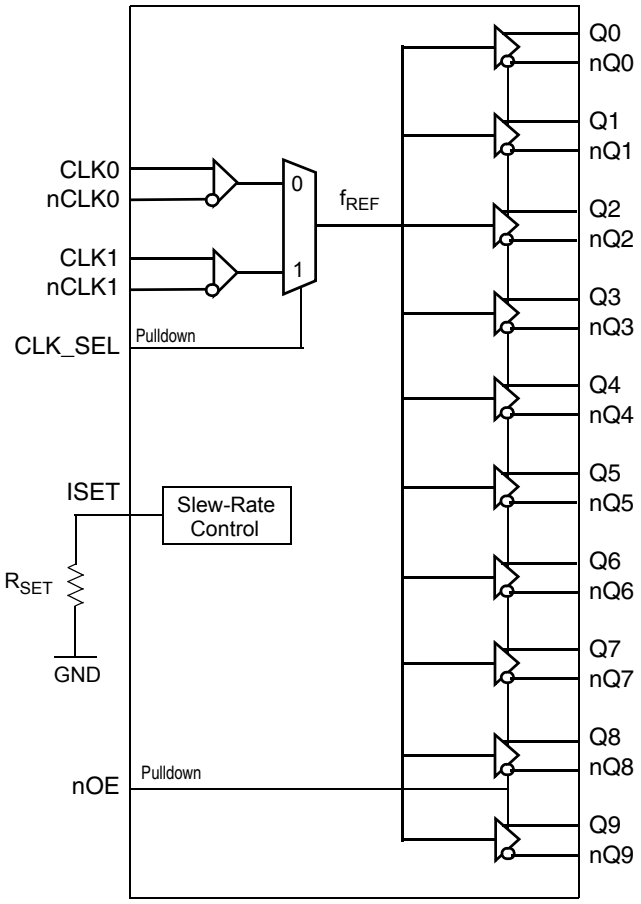
General Description

The ICS854110I is a high-performance differential LVDS clock fanout buffer. The device is designed for signal fanout of high-frequency, low phase-noise clock signals. The selected differential input signal is distributed to ten differential LVDS outputs. The ICS854110I is characterized to operate from a 2.5V power supply. Guaranteed output-to-output and part-to-part skew characteristics make the ICS854110I ideal for those clock distribution applications demanding well-defined performance and repeatability. The device offers an output slew rate control with four pre-set output transition times to solve crosstalk and EMI problems in complex board designs. A fail-safe input design forces the outputs to a defined state if differential clock inputs are open or shorted, see Table 3D.

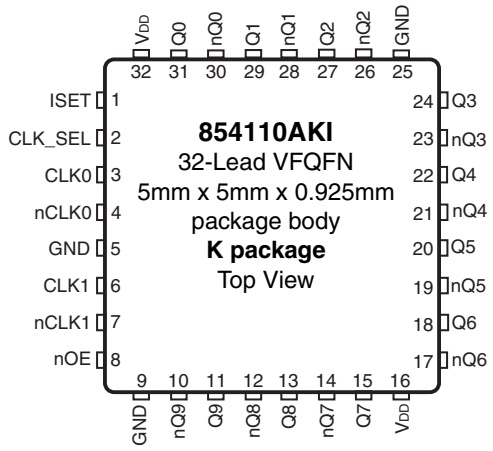
Features

- Two differential input reference clocks
- Differential pair can accept the following differential input levels: LVPECL, LVDS
- Ten LVDS outputs
- Maximum clock frequency: 200MHz
- Output slew rate control
- Fail-safe differential inputs
- LVCMOS interface levels for all control inputs
- Output skew: 260ps (maximum), for fastest slew rate setting of 0.650 V/ns
- Part-to-part skew: 1.2ns (maximum)
- Full 2.5V supply voltage
- Lead-free (RoHS 6) 32-Lead VFQFN and 32-Lead LQFP package
- -40°C to 85°C ambient operating temperature

Block Diagram



Pin Assignments



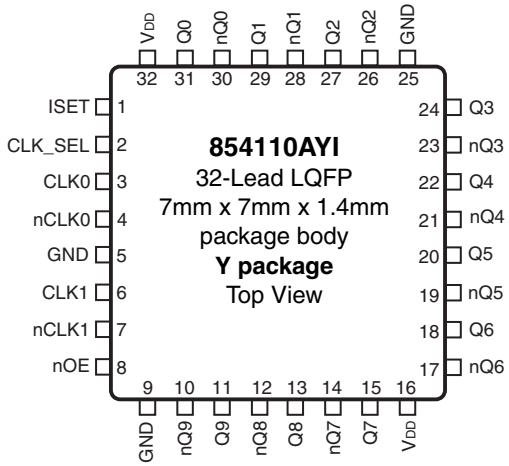


Table 1. Pin Descriptions

Number	Name	Type		Description
1	ISET			An external fixed resistor (RSET) from this pin to ground is needed to provide a reference current for setting the slew rate of the differential outputs Q[0:9], nQ[0:9]. See Table 3C for function.
2	CLK_SEL	Input	Pulldown	Input clock select. See Table 3A for function. LVCMOS/LVTTL interface levels.
3	CLK0	Input		Non-inverting clock/data input 0.
4	nCLK0	Input		Inverting differential clock input 0.
5, 9, 25	GND	Power		Power supply ground.
6	CLK1	Input		Non-inverting clock/data input 1.
7	nCLK1	Input		Inverting differential clock input 1.
8	nOE	Input	Pulldown	Output enable. See Table 3B for function. LVCMOS/LVTTL interface levels.
10, 11	nQ9, Q9	Output		Differential output pair 9. LVDS interface levels.
12, 13	nQ8, Q8	Output		Differential output pair 8. LVDS interface levels.
14, 15	nQ7, Q7	Output		Differential output pair 7. LVDS interface levels.
16, 32	V_{DD}	Power		Power supply pins.
17, 18	nQ6, Q6	Output		Differential output pair 6. LVDS interface levels.
19, 20	nQ5, Q5	Output		Differential output pair 5. LVDS interface levels.
21, 22	nQ4, Q4	Output		Differential output pair 4. LVDS interface levels.
23, 24	nQ3, Q3	Output		Differential output pair 3. LVDS interface levels.
26, 27	nQ2, Q2	Output		Differential output pair 2. LVDS interface levels.
28, 29	nQ1, Q1	Output		Differential output pair 1. LVDS interface levels.
30, 31	nQ0, Q0	Output		Differential output pair 0. LVDS interface levels.

NOTE: *Pulldown* refers to an internal input resistor. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 3A. CLK_SEL Configuration Table

Input	
CLK_SEL	Operation
0	CLK0, nCLK0 is the selected reference clock
1	CLK1, nCLK1 is the selected reference clock

NOTE: CLK_SEL is an asynchronous control.

Table 3B. nOE Configuration Table

Input	
nOE	Operation
0	Outputs Qx, nQx are enabled.
1	Outputs Qx, nQx are in high-impedance state.

NOTE: OE is an asynchronous control.

Table 3C. R_{SET} Configuration Table

R_{SET}	
Resistor Size (kΩ)	Typical Output Slew Rate (V/ns)
4	0.650 (fastest)
15	0.170
50	0.150
150	0.115 (slowest)

NOTE: The RSET resistor at the ISET pin allows configuration of the outputs to one of four pre-set output slew rates. A 5% variation of the RSET resistor size will be tolerated.
NOTE: Slew rates are defined as ±100mV from the center of Q – nQ signal.

Table 3D. Guaranteed Input Fail Safe Operations for CLK0, nCLK0 and CLK1, nCLK1

Input State of Selected Input	Outputs Q[0:9], nQ[0:9]
Logic Low (Selected Input: CLKx = LOW, nCLKx = HIGH)	Logic Low (Qx = LOW, nQx = HIGH)
Logic High (Selected Input: CLKx = HIGH, nCLKx = LOW)	Logic High (Qx = HIGH, nQx = LOW)
Inputs Open (Selected Input: CLKx = open, nCLKx = open)	Logic High (Qx = HIGH, nQx = LOW)
Inputs Shorted (Selected Input: CLKx shorted to nCLKx and tied to V_{DD})	Logic High (Qx = HIGH, nQx = LOW)
Input Shorted (Selected Input: CLKx shorted to nCLKx and floating)	Logic High (Qx = HIGH, nQx = LOW)

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O (LVDS) Continuos Current Surge Current	 10mA 15mA
Package Thermal Impedance, θ_{JA} 32 Lead VFQFN 32 Lead LQFP	 37.0°C/W (0 mps) 65.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current	No Load, R_{SET} not connected			18	mA
		All Outputs Loaded, R_{SET} = 4kΩ			86	mA
		No Load, R_{SET} = 4kΩ			30	mA

Table 4B. LVCMOS/LVTTL Input DC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	CLK_SEL, nOE	V_{DD} = V_{IN} = 2.625V			150	µA
I_{IL}	Input Low Current	CLK_SEL, nOE	V_{DD} = 2.625V, V_{IN} = 0V	-5			µA

Table 4C. Differential DC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1		0.15		1.2	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2		GND + 0.8		V_{DD} - 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as V_{IH}.

Table 4D. LVDS DC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage	R_{SET} = 4kΩ	250		600	mV
ΔV_{OD}	V_{OD} Magnitude Change	R_{SET} = 4kΩ			50	mV
V_{OS}	Offset Voltage	R_{SET} = 4kΩ	1.115		1.430	V
ΔV_{OS}	V_{OS} Magnitude Change	R_{SET} = 4kΩ			50	mV

AC Electrical Characteristics

Table 5. AC Electrical Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

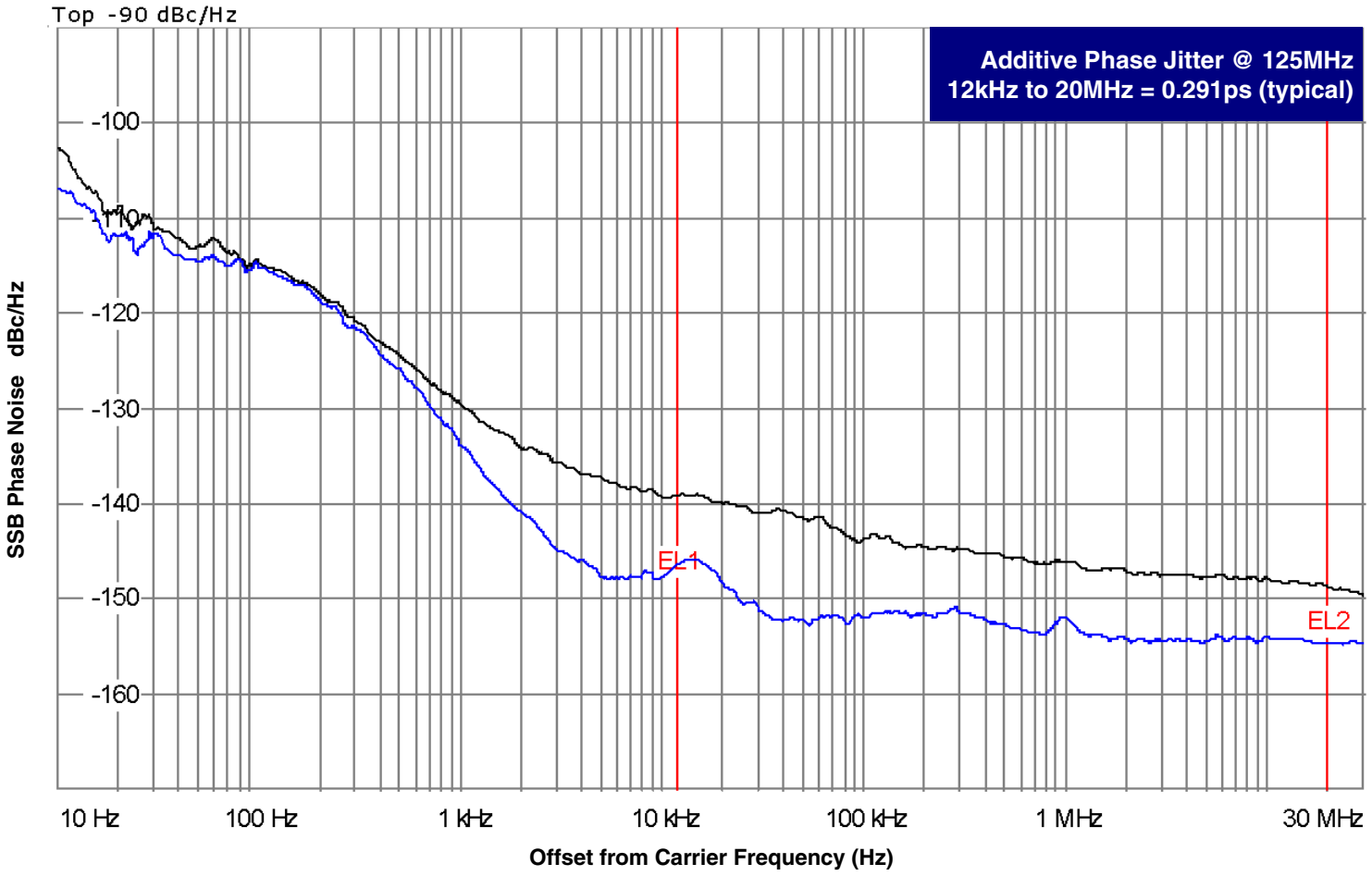
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{REF}	Input Frequency		R_{SET} = 4kΩ			200	MHz
			R_{SET} = 15kΩ			30	MHz
			R_{SET} = 50kΩ			20	MHz
			R_{SET} = 150kΩ			16	MHz
f_{OUT}	Output Frequency	Q[9:0], nQ[9:0]	R_{SET} = 4kΩ			200	MHz
			R_{SET} = 15kΩ			30	MHz
			R_{SET} = 50kΩ			20	MHz
			R_{SET} = 150kΩ			16	MHz
t_{JIT}	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section		R_{SET} = 4kΩ, f_{REF} = 125MHz, Integration Range: 12kHz – 20MHz		0.291		ps
t_{PD}	Propagation Delay; NOTE 1	CLKx, nCLKx to any Qx, nQx output	R_{SET} = 4kΩ	3.2	4.0	4.6	ns
			R_{SET} = 15kΩ	4.6	5.5	6.3	ns
			R_{SET} = 50kΩ	5.4	6.5	7.7	ns
			R_{SET} = 150kΩ	7.5	8.3	9.3	ns
*t*sk(o)	Output Skew; NOTE 2, 3		R_{SET} = 4kΩ		125	260	ps
			R_{SET} = 15kΩ		160	425	ps
			R_{SET} = 50kΩ		200	525	ps
			R_{SET} = 150kΩ		240	550	ps
*t*sk(p)	Pulse Skew		R_{SET} = 4kΩ		80	185	ps
			RSET ≠ 4kΩ			265	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4		R_{SET} = 4kΩ		600	1200	ps
			R_{SET} = 15kΩ		825	1500	ps
			R_{SET} = 50kΩ		975	2100	ps
			R_{SET} = 150kΩ		1245	1650	ps
*t*sl(o)	Output Clock Slew Rate		R_{SET} = 4kΩ	0.450	0.650	1.3	V/ns
			R_{SET} = 15kΩ	0.110	0.170	0.350	V/ns
			R_{SET} = 50kΩ	0.110	0.150	0.325	V/ns
			R_{SET} = 150kΩ	0.075	0.115	0.250	V/ns
odc	Output Duty Cycle; NOTE 5		R_{SET} = 4kΩ, f_{REF} ≤ 200MHz	45	50	55	%
			R_{SET} = 15kΩ, f_{REF} ≤ 30MHz	48	50	52	%
			R_{SET} = 50kΩ, f_{REF} ≤ 20MHz	48	50	52	%
			R_{SET} = 150kΩ, f_{REF} ≤ 16MHz	48	50	52	%

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
t_R / t_F	Output Rise/ Fall Time; 30% to 70%	R_{SET} = 4kΩ	100	300	500	ps
		R_{SET} = 15kΩ	600	1030	1600	ps
		R_{SET} = 50kΩ	650	1160	1850	ps
		R_{SET} = 150kΩ	800	1540	2200	ps

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 5: Input Duty Cycle must be 50%.

Additive Phase Jitter

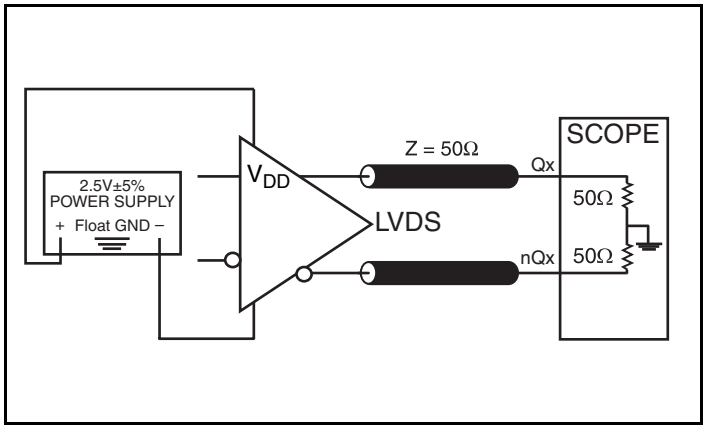
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



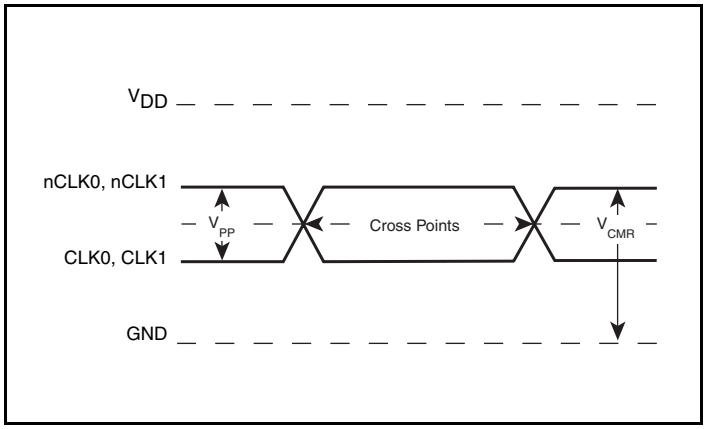
As with most timing specifications, phase noise measurements have issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

The source generator used is, "Rohde & Schwarz SMA 100A Signal Generator into a HP 8133A 3GHz Pulse Generator".

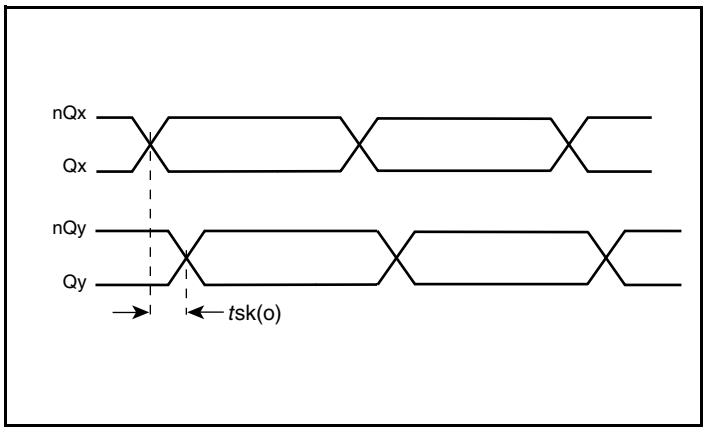
Parameter Measurement Information



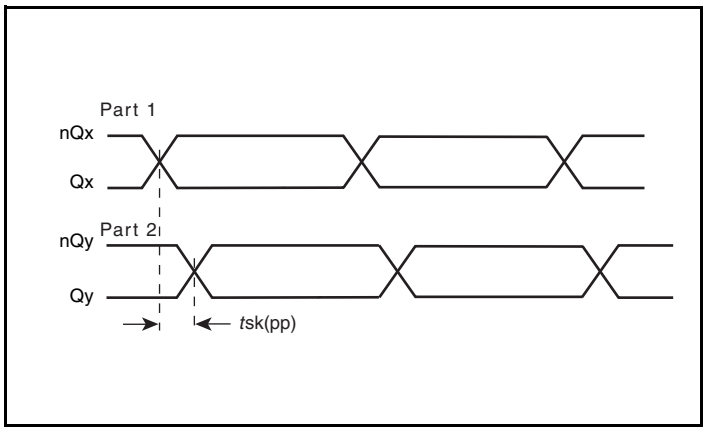
2.5V LVDS Output Load AC Test Circuit



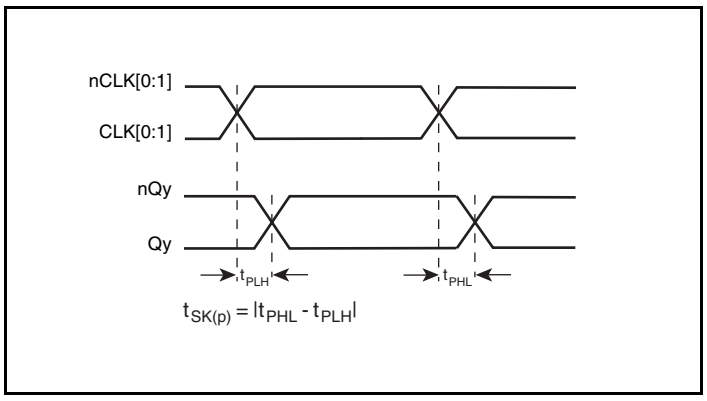
Differential Input Level



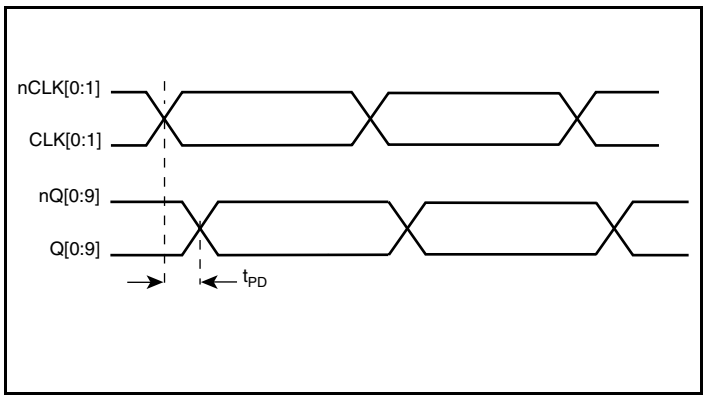
Output Skew



Part-to-Part Skew

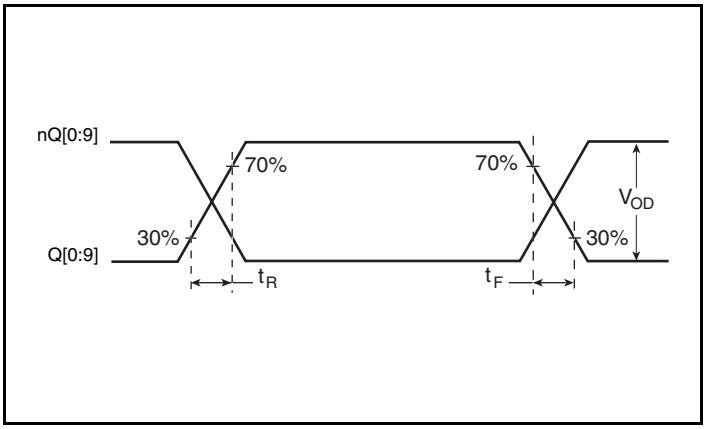


Pulse Skew

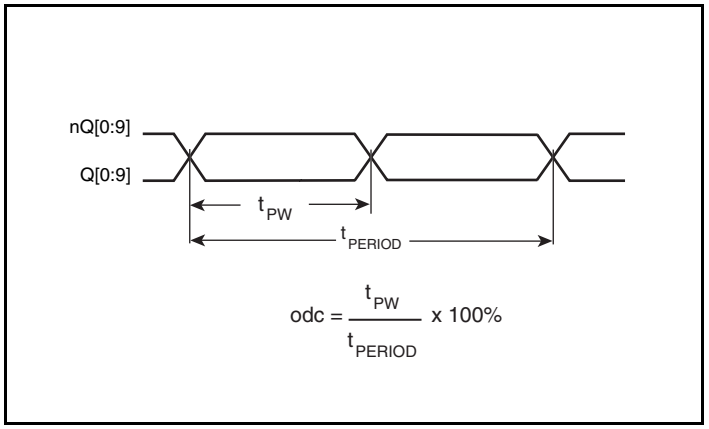


Propagation Delay

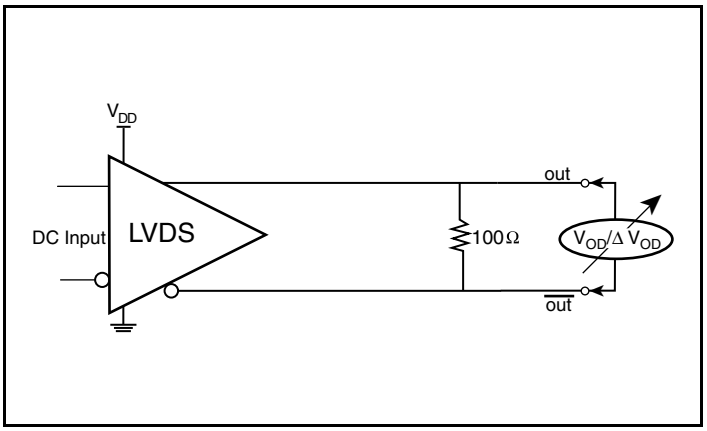
Parameter Measurement Information, continued



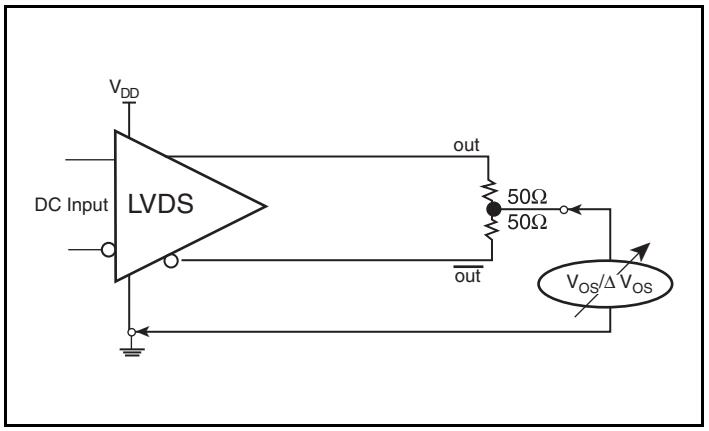
Output Rise/Fall Time



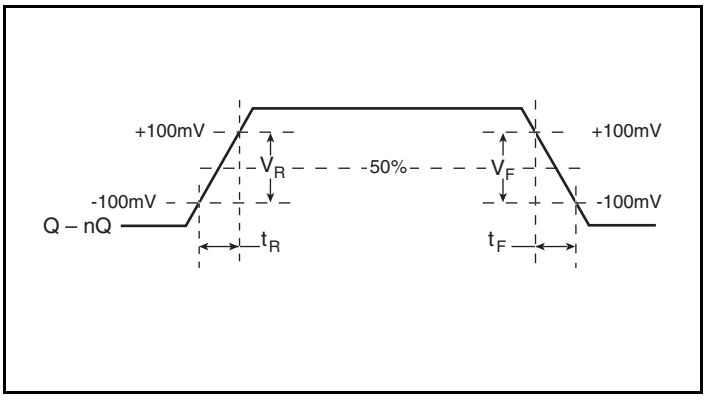
Output Duty Cycle/Pulse Width/Period



Differential Output Voltage Setup



Offset Voltage Setup



Differential Output Slew Rate

Applications Information

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{DD} = 3.3V, R1 and R2 value should be adjusted to set V_{REF} at 1.25V. The values below are for when both the single ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{DD} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

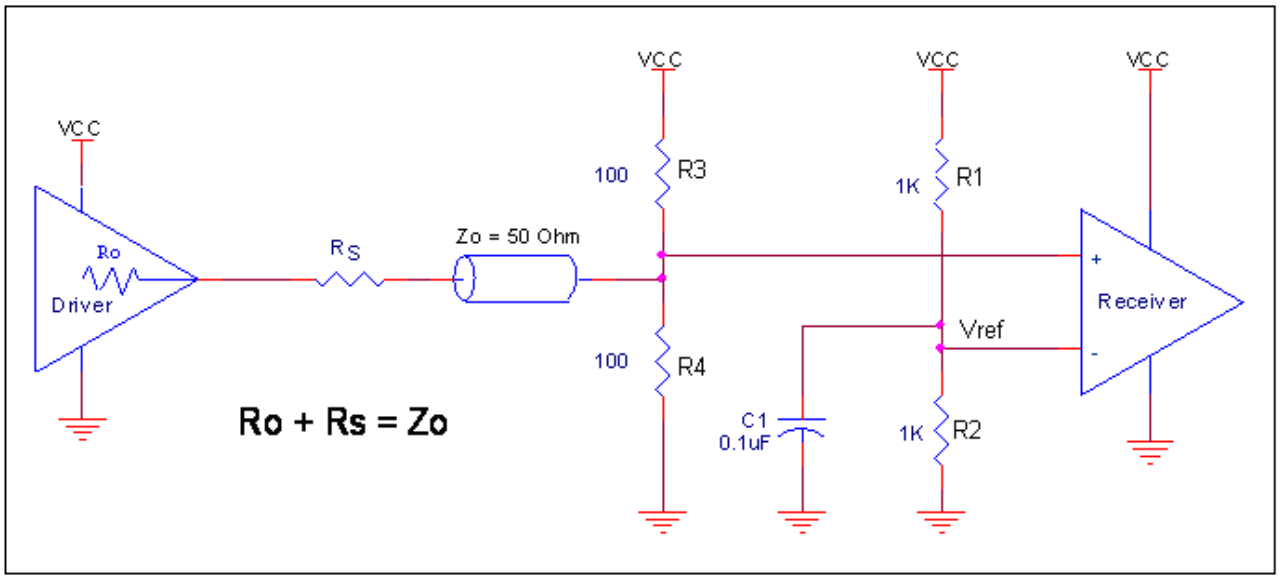


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

Recommendations for Unused Input and Output Pins

Inputs:

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVDS Outputs

All unused LVDS outputs should be terminated with 100Ω resistor between the differential pair.

Differential Clock Input Interface

The CLK/nCLK accepts LVPECL, LVDS and other differential signals. Both differential signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2C* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

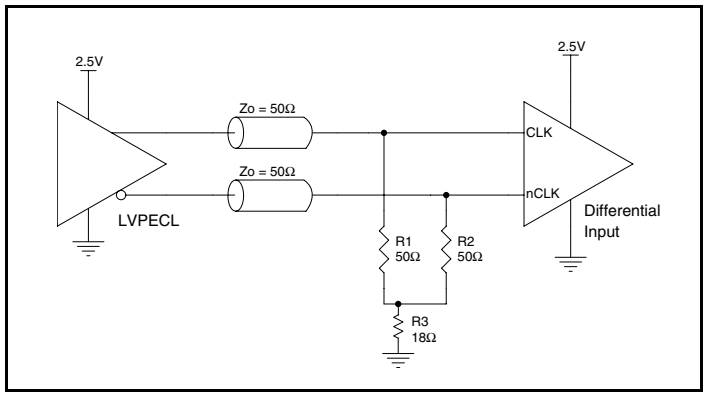


Figure 2A. CLK/nCLK Input Driven by a 2.5V LVPECL Driver

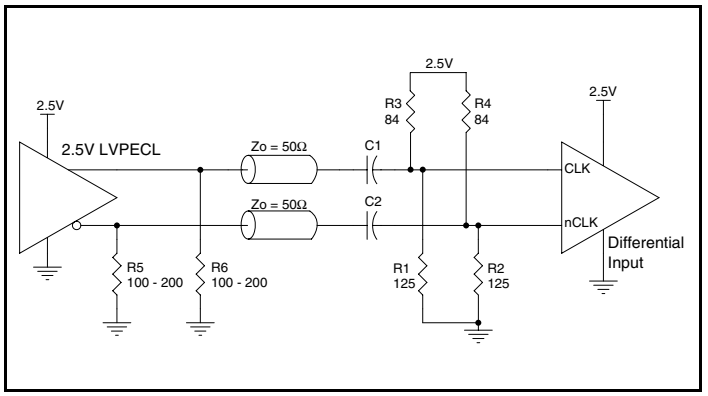


Figure 2B. CLK/nCLK Input Driven by a 2.5V LVPECL Driver with AC Coupler

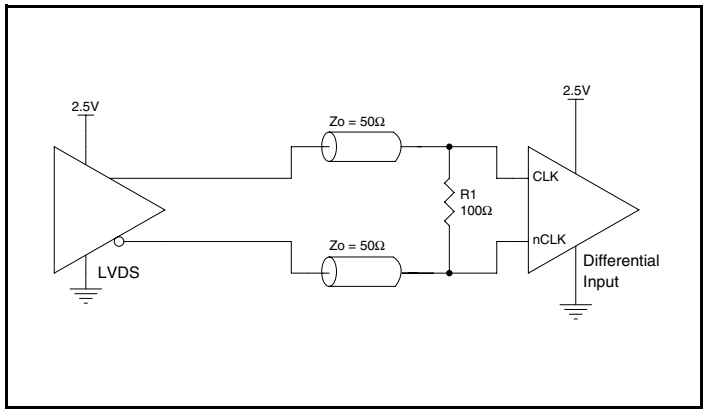


Figure 2C. CLK/nCLK Input Driven by an LVDS Driver

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 3.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

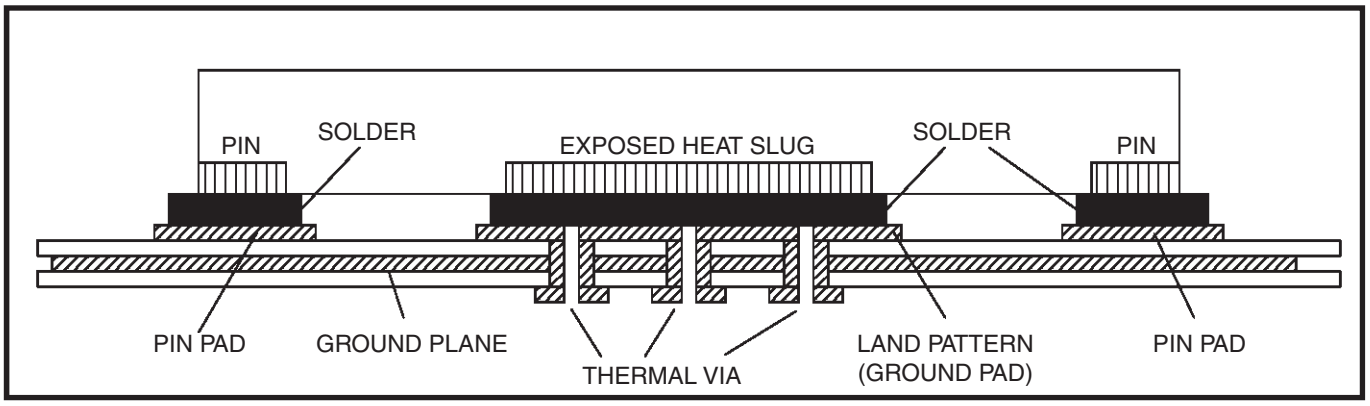


Figure 3. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

LVDS Driver Termination

A general LVDS interface is shown in *Figure 4*. Standard termination for LVDS type output structure requires both a 100Ω parallel resistor at the receiver and a 100Ω differential transmission line environment. In order to avoid any transmission line reflection issues, the 100Ω resistor must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in Figure 4 can be used with either type of output structure. If using a non-standard termination, it is recommended to contact IDT and confirm if the output is a current source or a voltage source type structure. In addition, since these outputs are LVDS compatible, the amplitude and common mode input range of the input receivers should be verified for compatibility with the output.

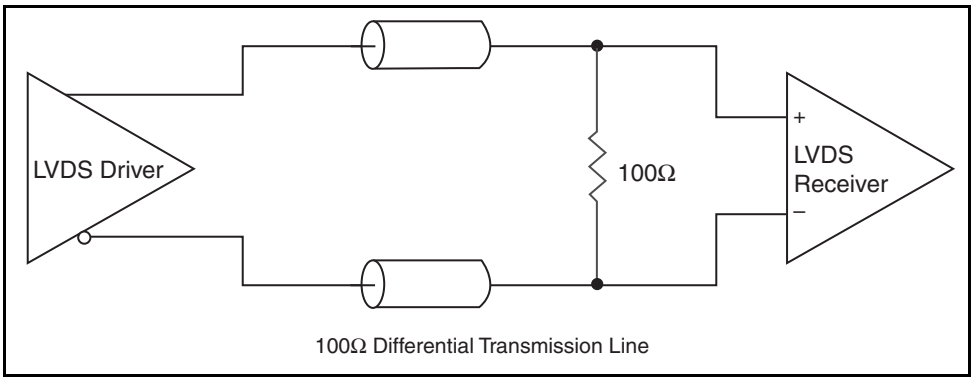


Figure 4. Typical LVDS Driver Termination

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS854110I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS54110I is the sum of the core power plus the power dissipation in the load(s).
The following is the power dissipation for V_{DD} = 2.5V + 5% = 2.625V, which gives worst case results.

Total power dissipation, includes power dissipation on external components.

- P_core+load = V_{DD_MAX} * $I_{DD\_core+load}$ = 2.625V * 86mA = **225.75mW**

  Where:
  $I_{DD\_core+load}$ is the total supply current which includes external components

To calculate the power dissipation on the device alone, Pd_total, and use it for junction temperature calculation, subtract the power dissipation on the external components.

- Pd_total = P_core+load – (P_load + P_rset)

  Where:
  P_load is power dissipation on the output loadings
  P_rset is power dissipation on the R_{SET}

The load current per output is:

- Iout = ($I_{DD\_core+load}$ – $I_{DD\_no\_load}$) / N = (86mA – 18mA) / 10 = **6.8mA**

  Where:
  $I_{DD\_no\_load}$ is I_{DD} current at no load condition
  N is number of outputs

Power Dissipation on output loads

- P_load = (Iout)^2 * R_load * N = (6.8mA)^2 * 100Ω * 10 = **46.2mW**

Power Dissipation on R_{SET}

- P_rset = (Vrset)^2 / R_{SET} = (1V)^2 / 4kΩ = **0.25mW**
  (NOTE: P_rset is small and can be negligible)

Total Power Dissipation on the part excluding the power dissipation on the external components.

Pd_total = P_core+load – (P_load + P_rset)
= 225.75mW – (46.2mW + 0.25mW)
= 179.3mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 65.7°C/W per Table 6A below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.179W * 65.7°C/W = 96.8°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6A. Thermal Resistance θ_{JA} for 32 Lead LQFP, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	65.7°C/W	55.9°C/W	52.4°C/W

Table 6B. Thermal Resistance θ_{JA} for 32 Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29.0°C/W

Reliability Information

Table 7A. θ_{JA} vs. Air Flow Table for a 32-Lead VFQFN

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29.0°C/W

Table 7B. θ_{JA} vs. Air Flow Table for a 32-Lead LQFP

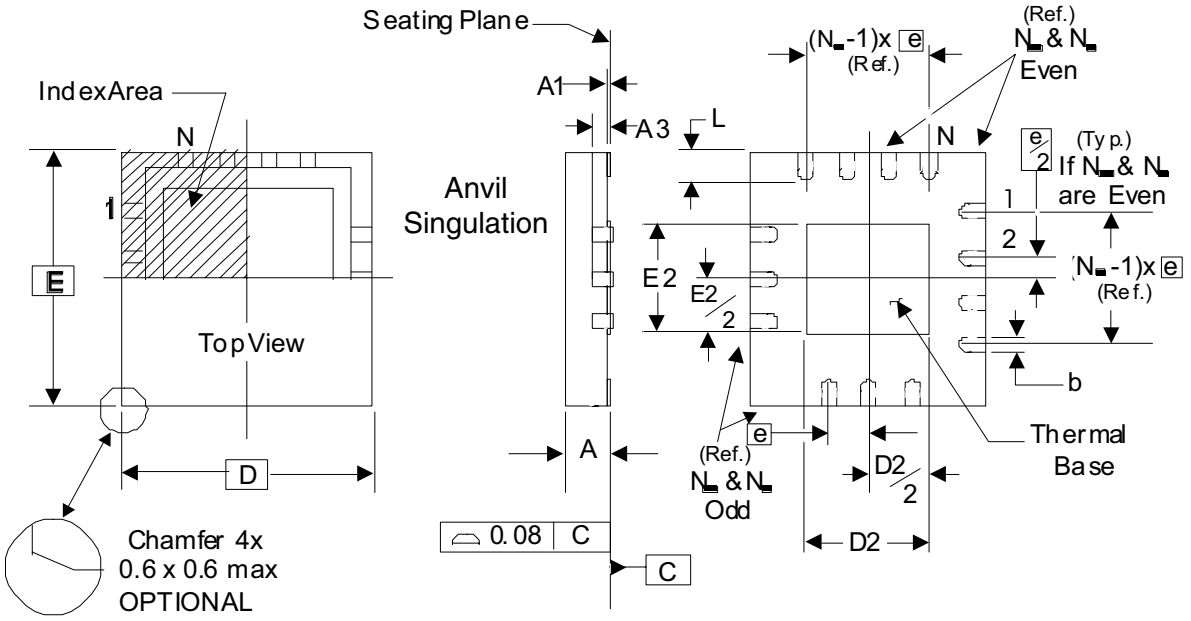
θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	65.7°C/W	55.9°C/W	52.4°C/W

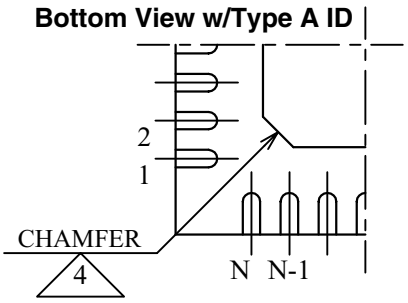
Transistor Count

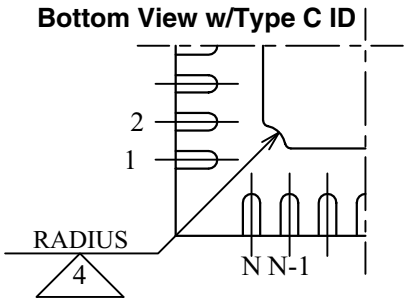
The transistor count for ICS854110I is: 1757

Package Outline and Package Dimensions

Package Outline - K Suffix for 32-Lead VFQFN







There are 2 methods of indicating pin 1 corner at the back of the VFQFN package are:

1. Type A: Chamfer on the paddle (near pin 1)
2. Type C: Mouse bite on the paddle (near pin 1)

Table 8A. Package Dimensions for 32-Lead VFQFN

JEDEC Variation: VHHD-2/-4 All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	32	
A	0.80	1.00
A1	0	0.05
A3	0.25 Ref.	
b	0.18	0.30
N_D & N_E		8
D & E	5.00 Basic	
D2 & E2	3.0	3.3
e	0.50 Basic	
L	0.30	0.50

Reference Document: JEDEC Publication 95, MO-220

NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 8A.

Package Outline and Package Dimensions

Package Outline - Y Suffix for 32-Lead LQFP

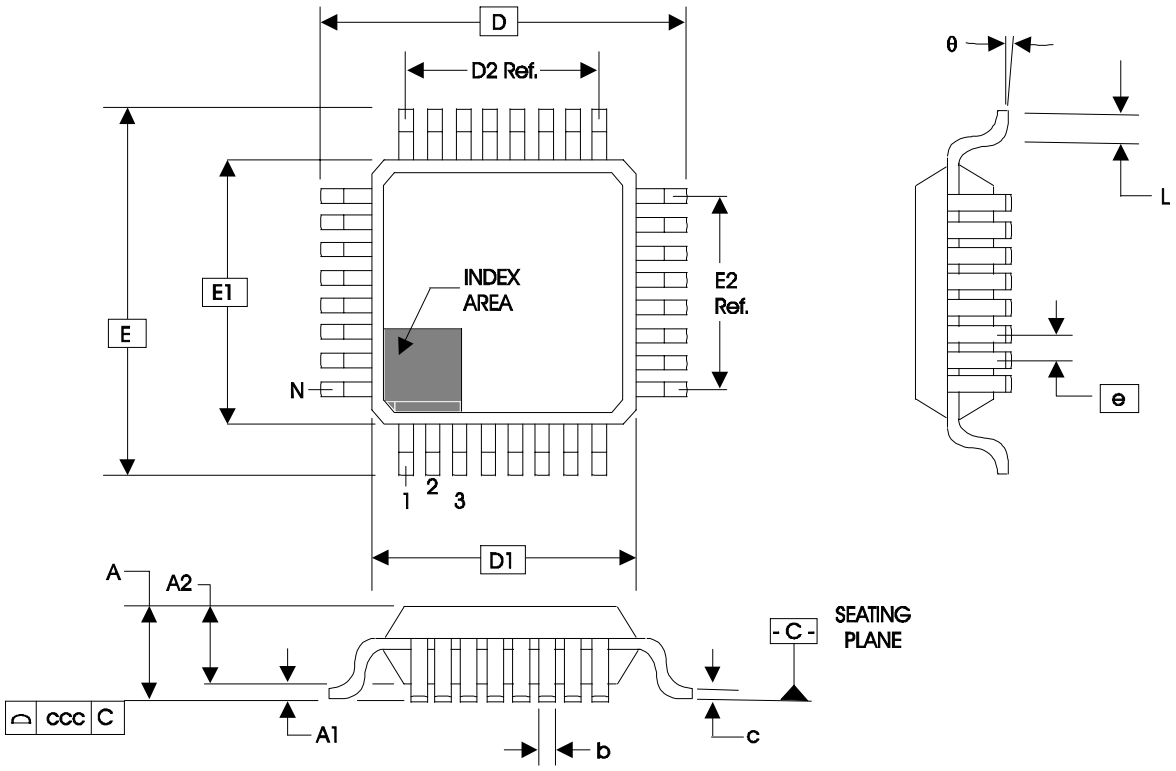


Table 8B. Package Dimensions 32 Lead LQFP

JEDEC Variation: BBA All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		32	
A			1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
b	0.30		0.45
c	0.09		0.20
D & E		9.00 Basic	
D1 & E1		7.00 Basic	
e		0.80 Basic	
L	0.45	0.60	0.75
θ	0°		7°
ccc			0.10

Reference Document: JEDEC Publication 95, MS-026

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
854110AKILF	ICS54110AIL	“Lead-Free” 32 Lead VFQFN	Tray	-40°C to 85°C
854110AKILFT	ICS54110AIL	“Lead-Free” 32 Lead VFQFN	2500 Tape & Reel	-40°C to 85°C
854110AYILF	ICS854110AIL	“Lead-Free” 32 Lead LQFP	Tray	-40°C to 85°C
854110AYILFT	ICS854110AIL	“Lead-Free” 32 Lead LQFP	1000 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an “LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
B	T4A	4	Power Supply DC Characteristics Table - added I_{DD} spec of 30mA max.	1/27/11

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